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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV

ECN

DESCRIPTION OF REVISION

CK APPD
DATE

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0003549590

ENGINEERING RELEASED

2014-12-19

X304 MLB SCHEMATIC - DVT

Fri Dec 19 12:14:48 2014

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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-1573	1	SCHEM,MLB,X304	SCH	CRITICAL	
820-4924	1	PCBF,MLB,X304	PCB	CRITICAL	

DRAWING TITLE

SCHEM,MLB,X304

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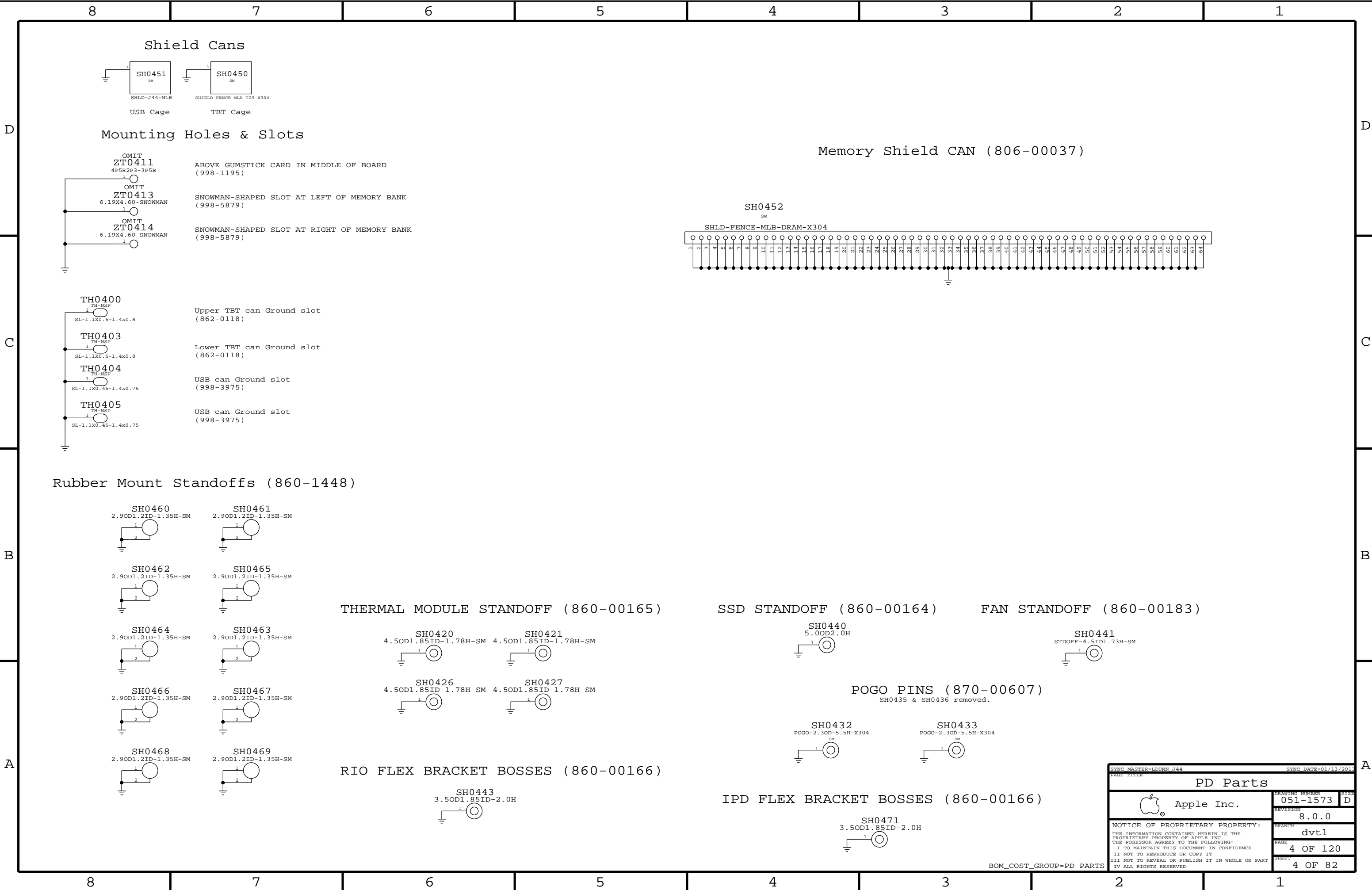
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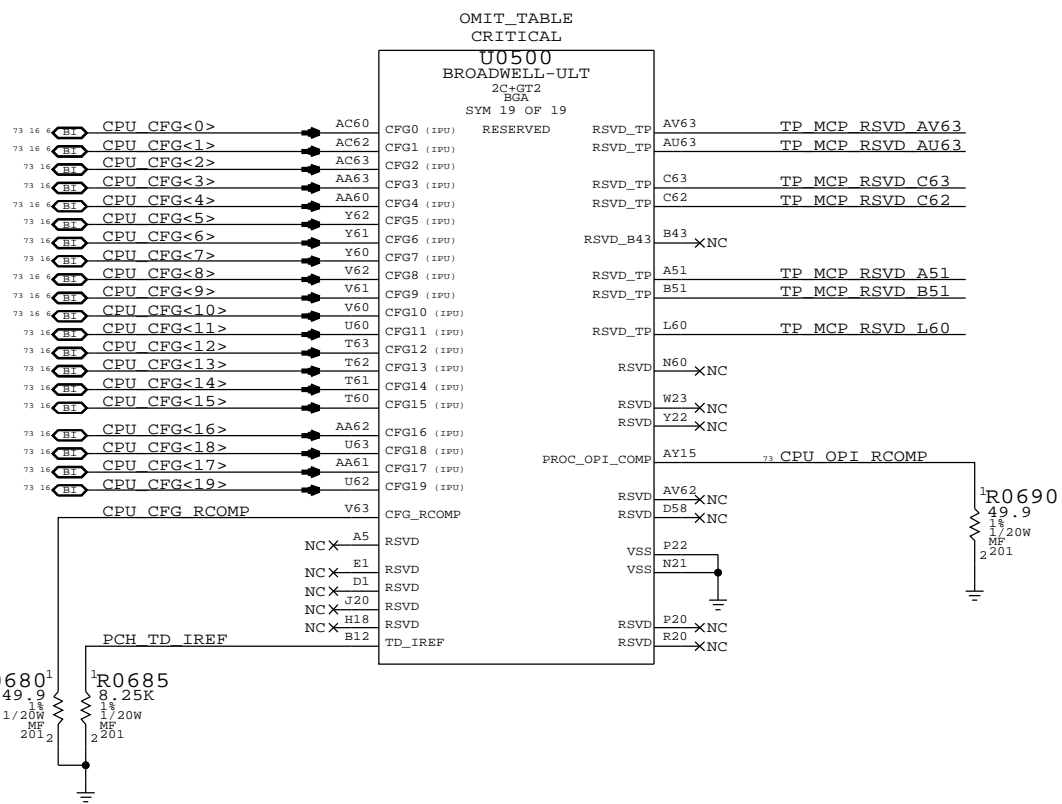
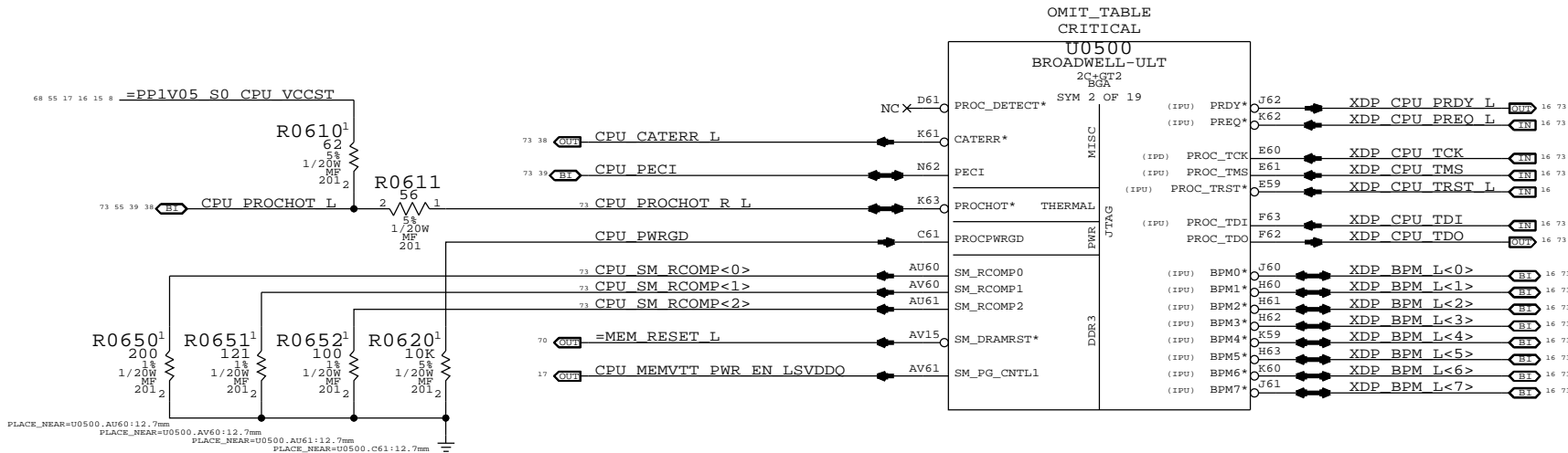
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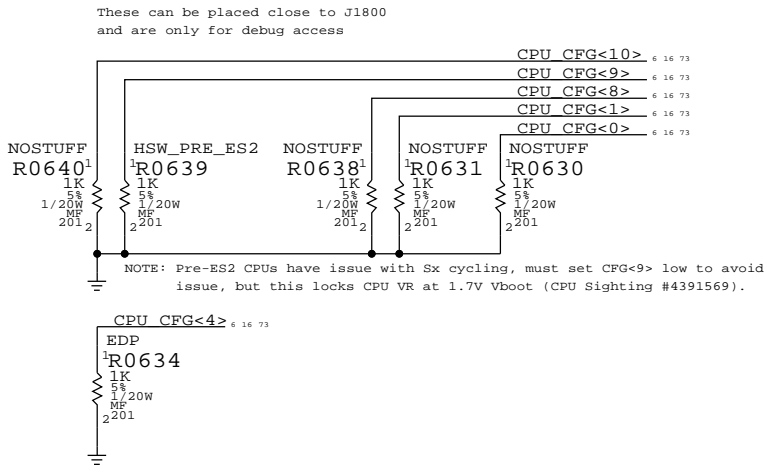
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CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE
CFG<9>:NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID
CFG<8>:ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED
CFG<4>:eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG<1>:PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE
CFG<0>:RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK



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SYNC DATE=10/23/2012

CPU Misc,JTAG,CFG,RSVD

Apple Inc.

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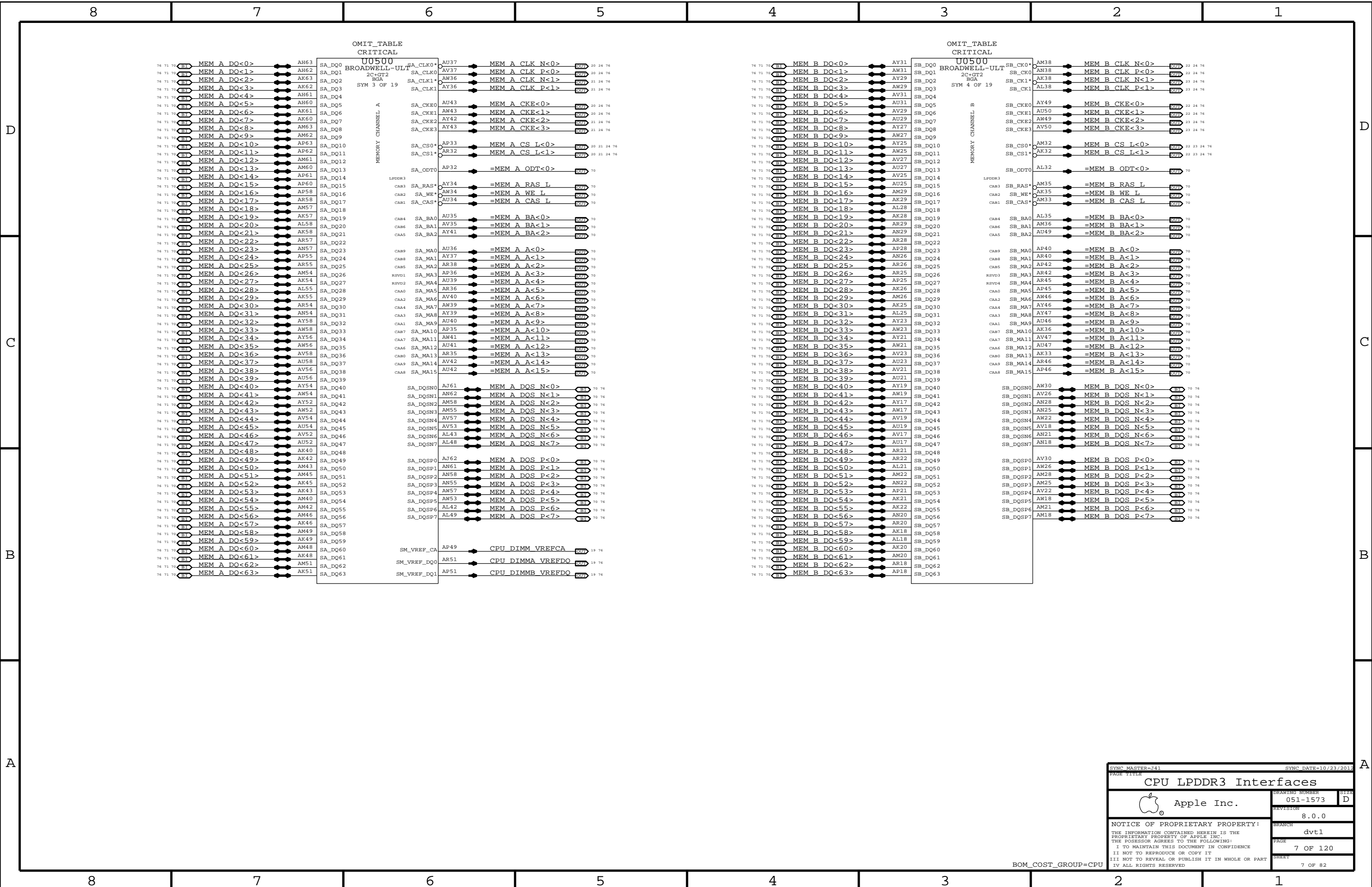
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CPU LPDDR3 Interfaces

Apple Inc.

DRAWING NUMBER051-1573

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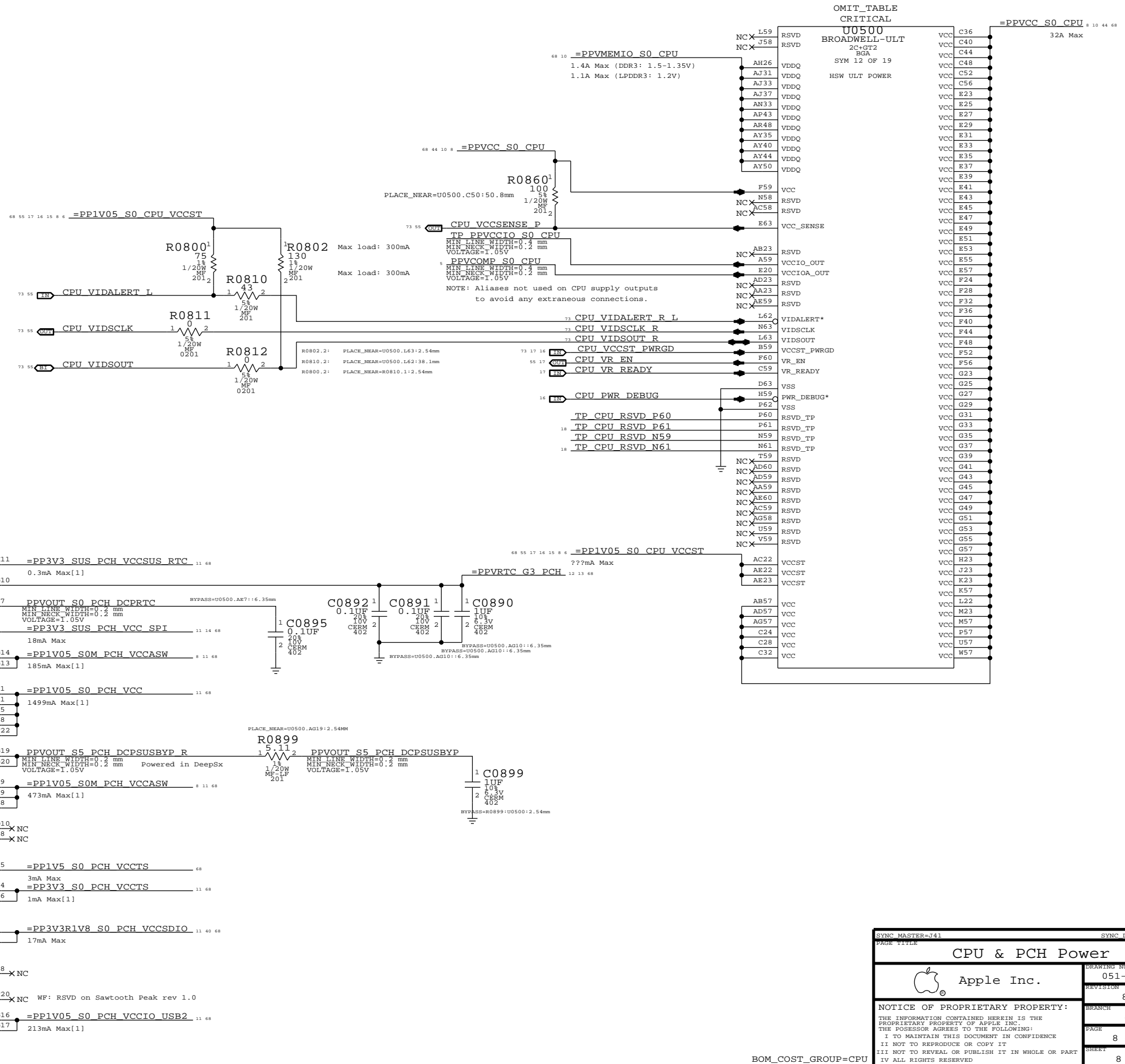
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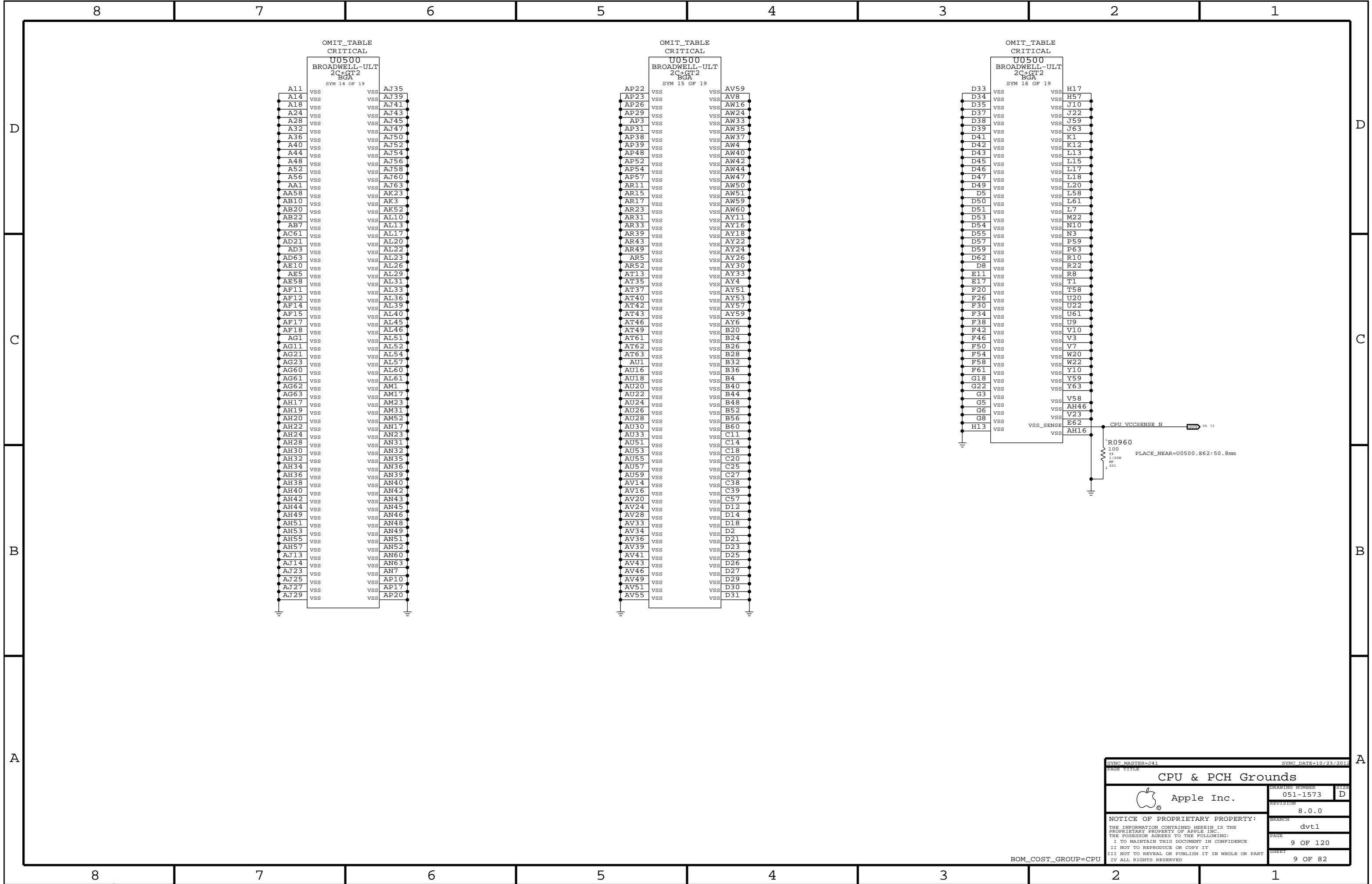
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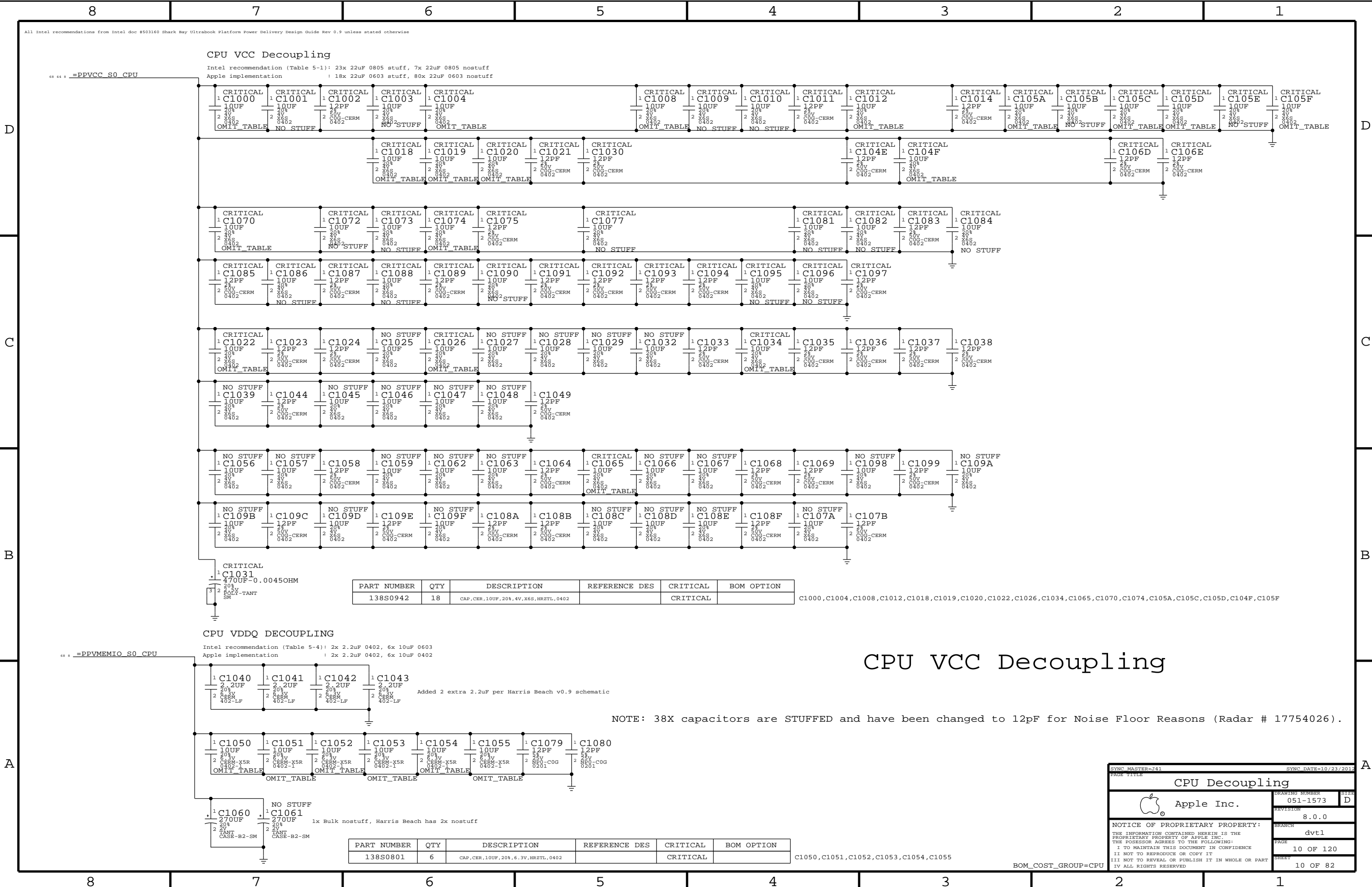
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BDW-ULT current estimates from Broadwell Mobile ULT Processor EDS vol.1 Doc# 514405, Rev.: 0.9v1
Wildcat Point-LP current estimates from Wildcat Point-LP PCH EDS, Doc# 515621, Rev. 0.9
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.




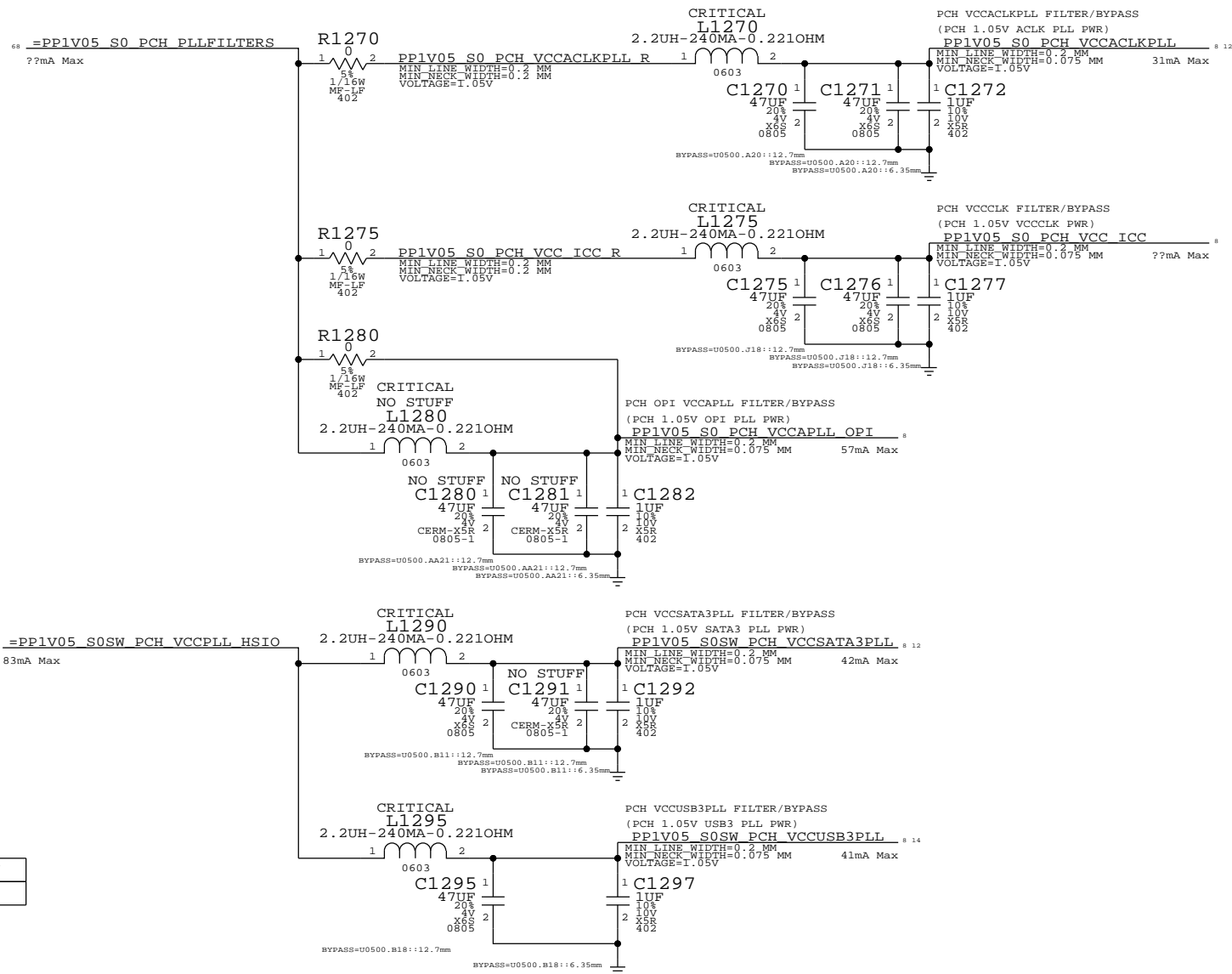
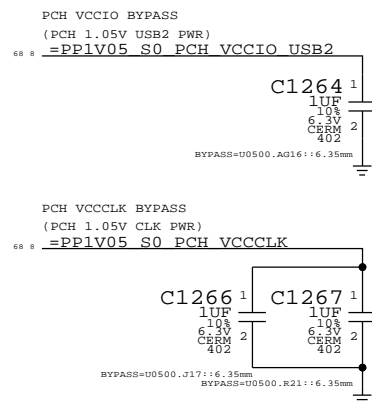
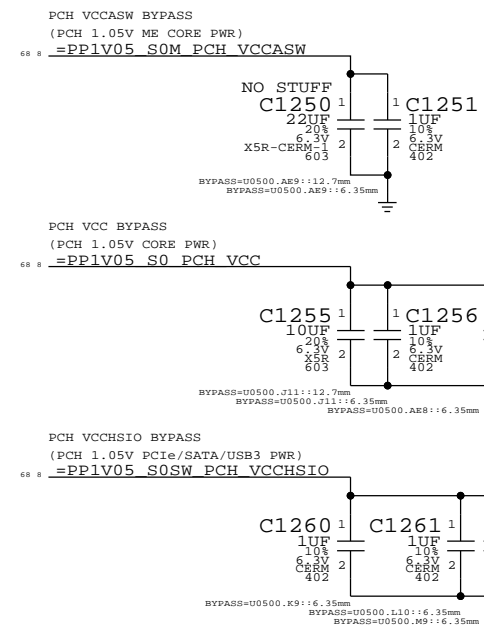
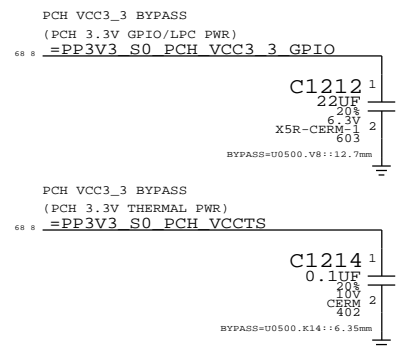
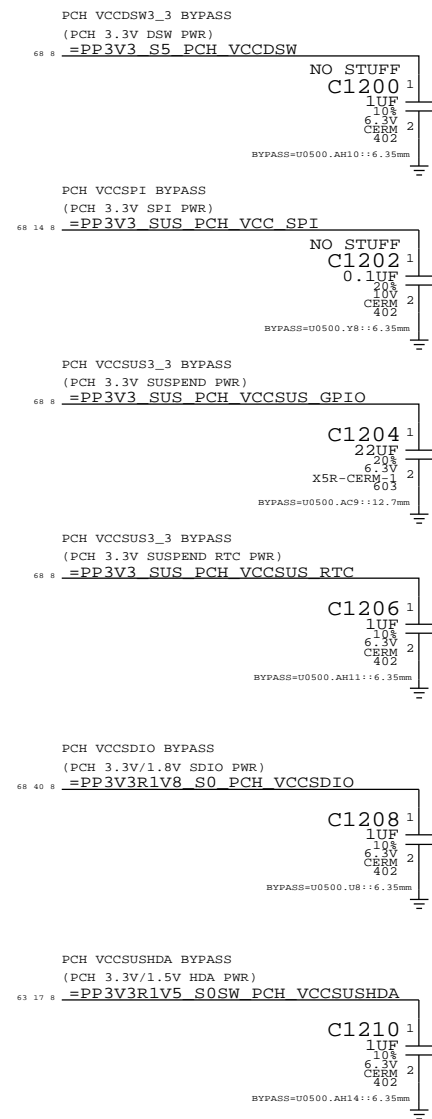
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CPU VCC Decoupling


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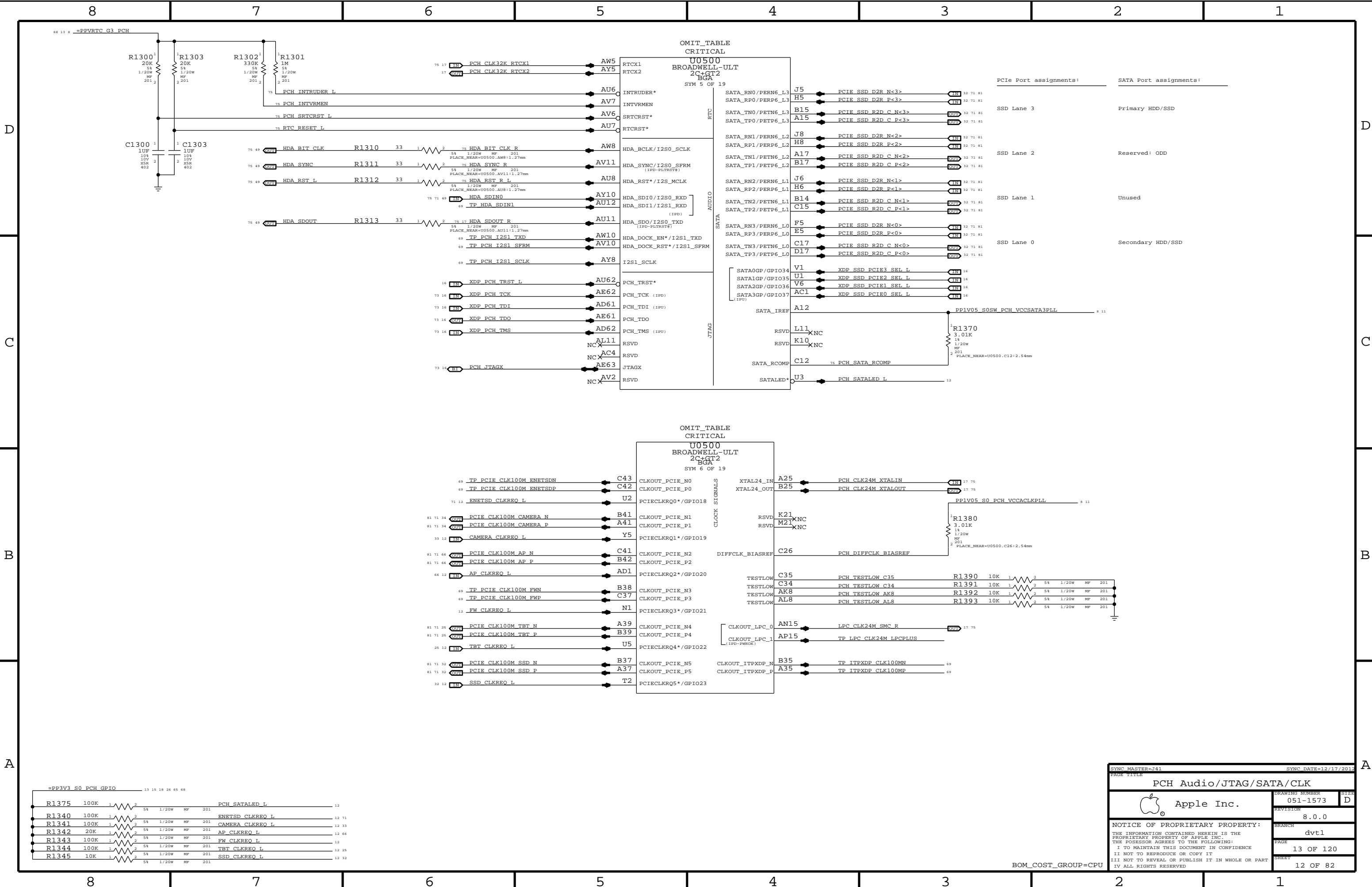


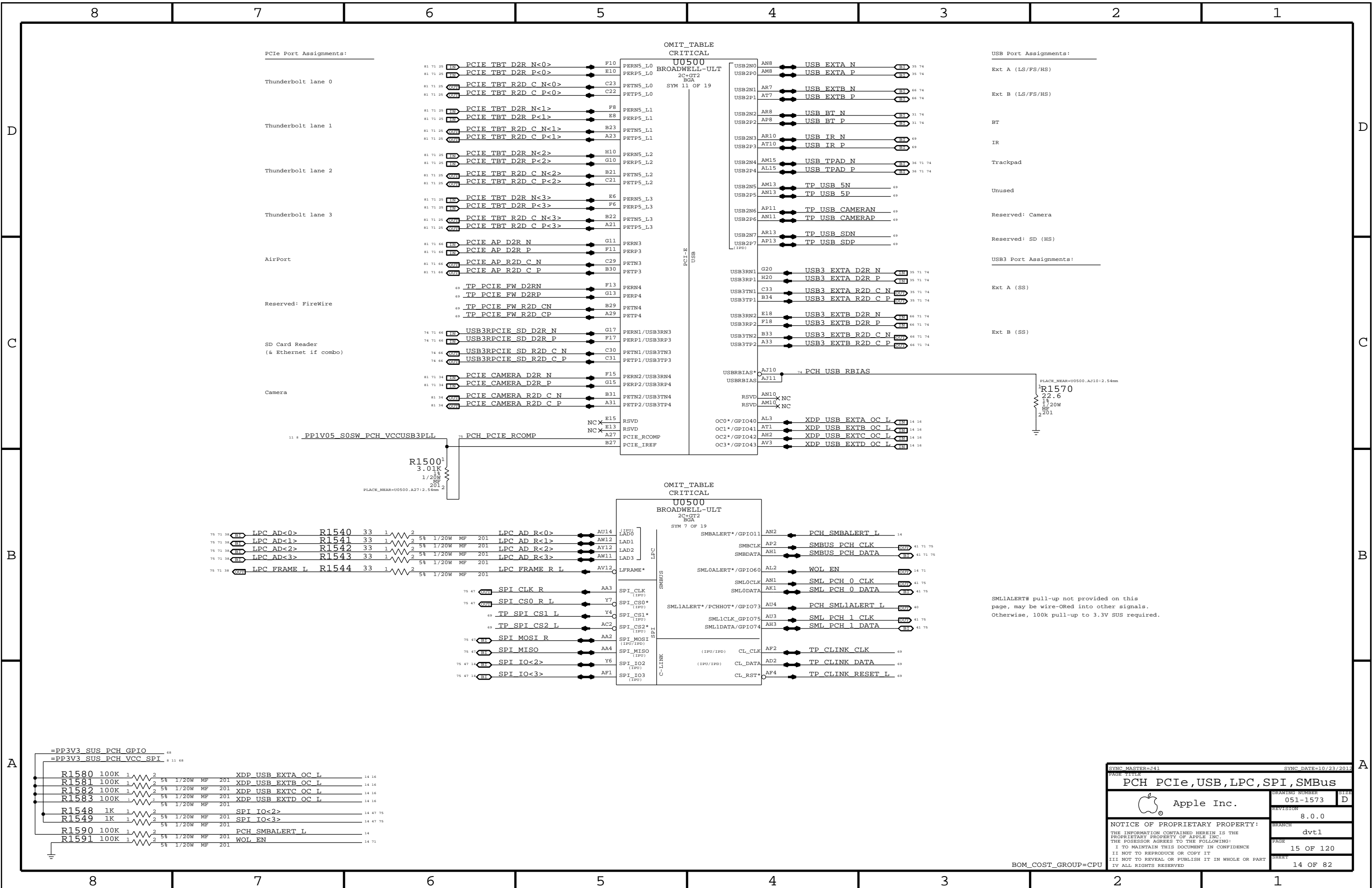
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138S0801	1	CAP, CER, 10UF, 20%, 6.3V, HRZTL, 0402	C1262	CRITICAL	

Wildcat Point-LP current estimates from Wildcat Point-LP PCH EDS, Doc# 515621, Rev. 0.9 as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

BOM COST GROUP=CPU

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PCH PCie,USB,LPC,SPI,SMBus

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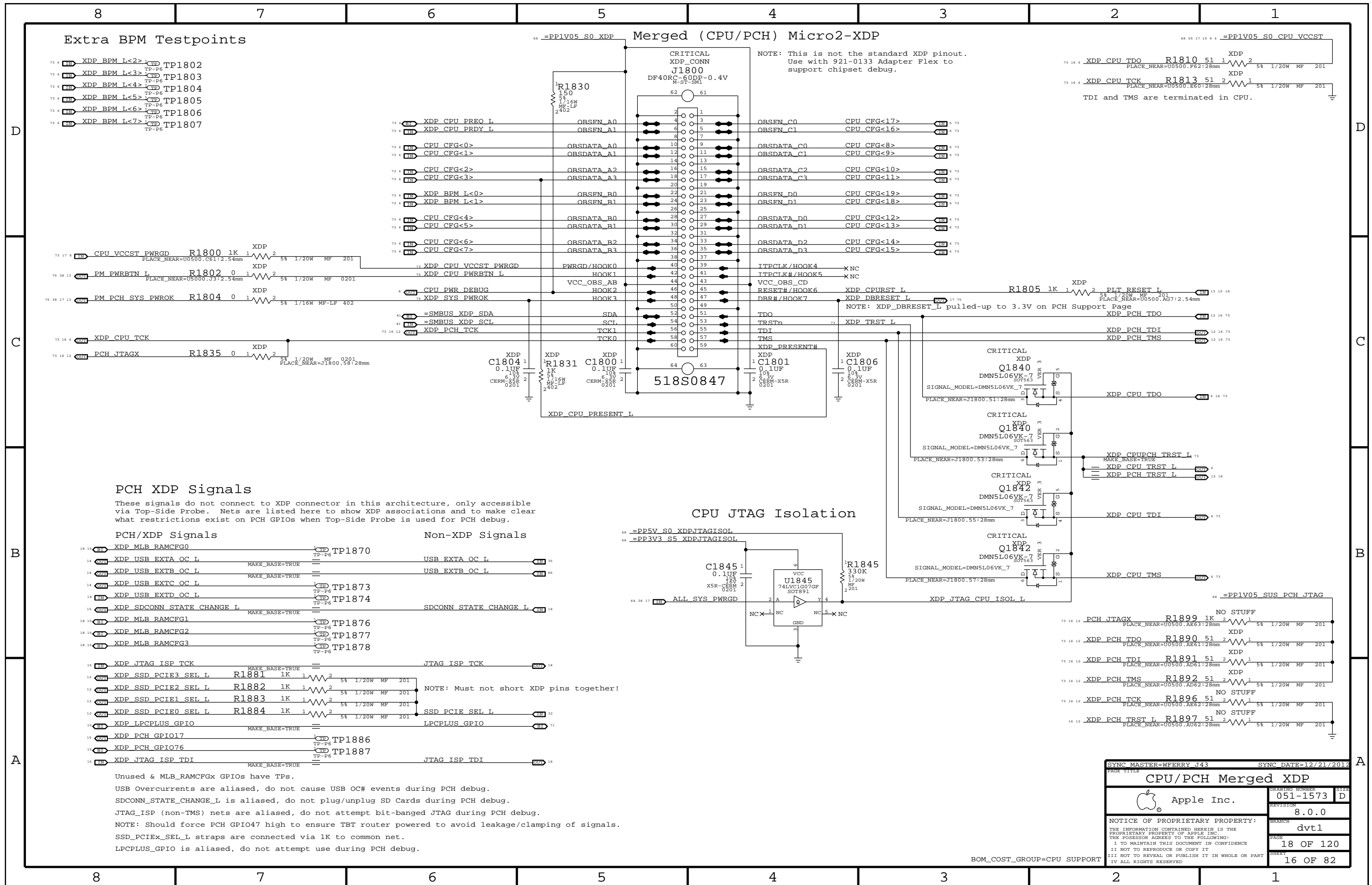
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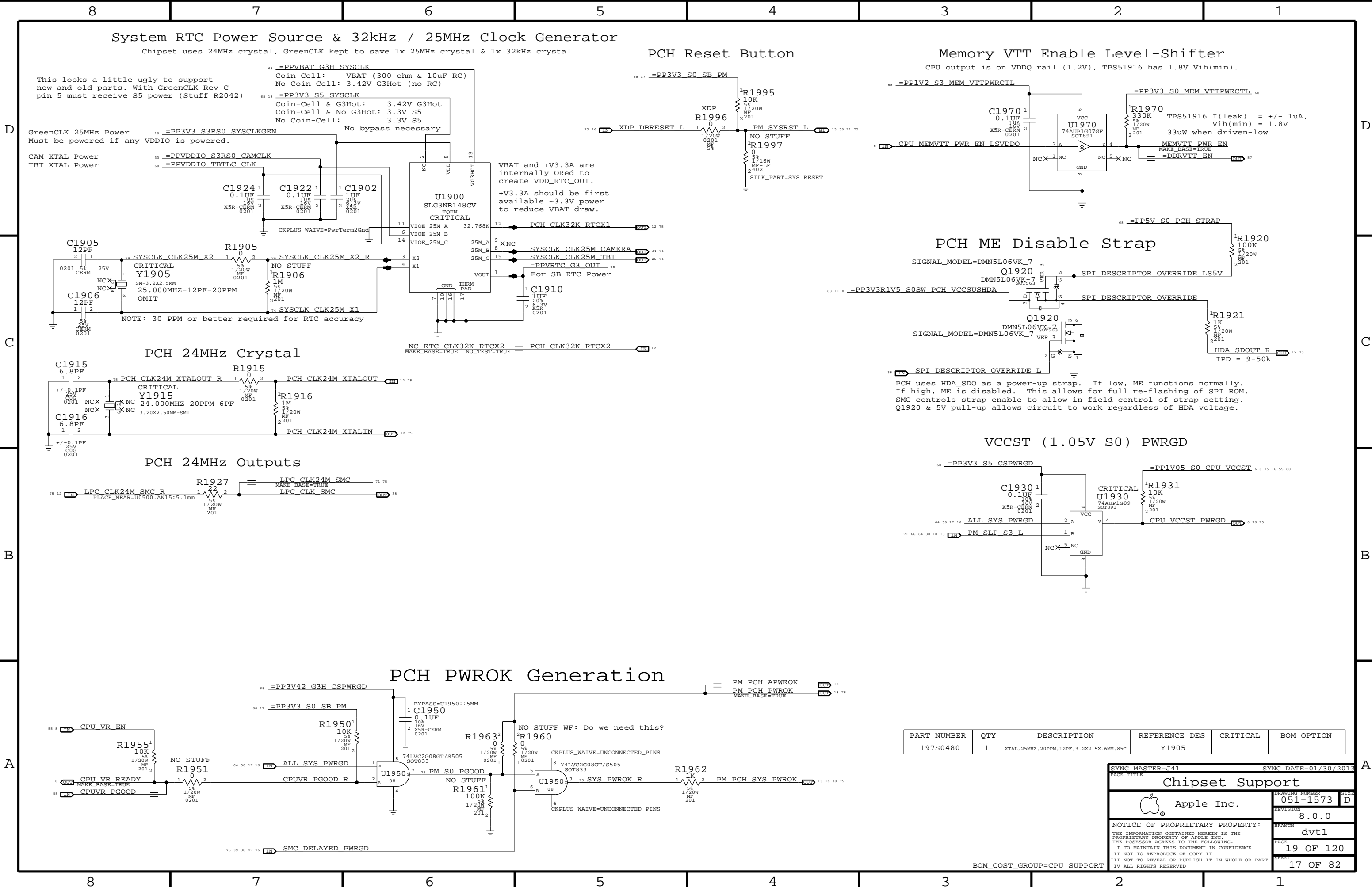
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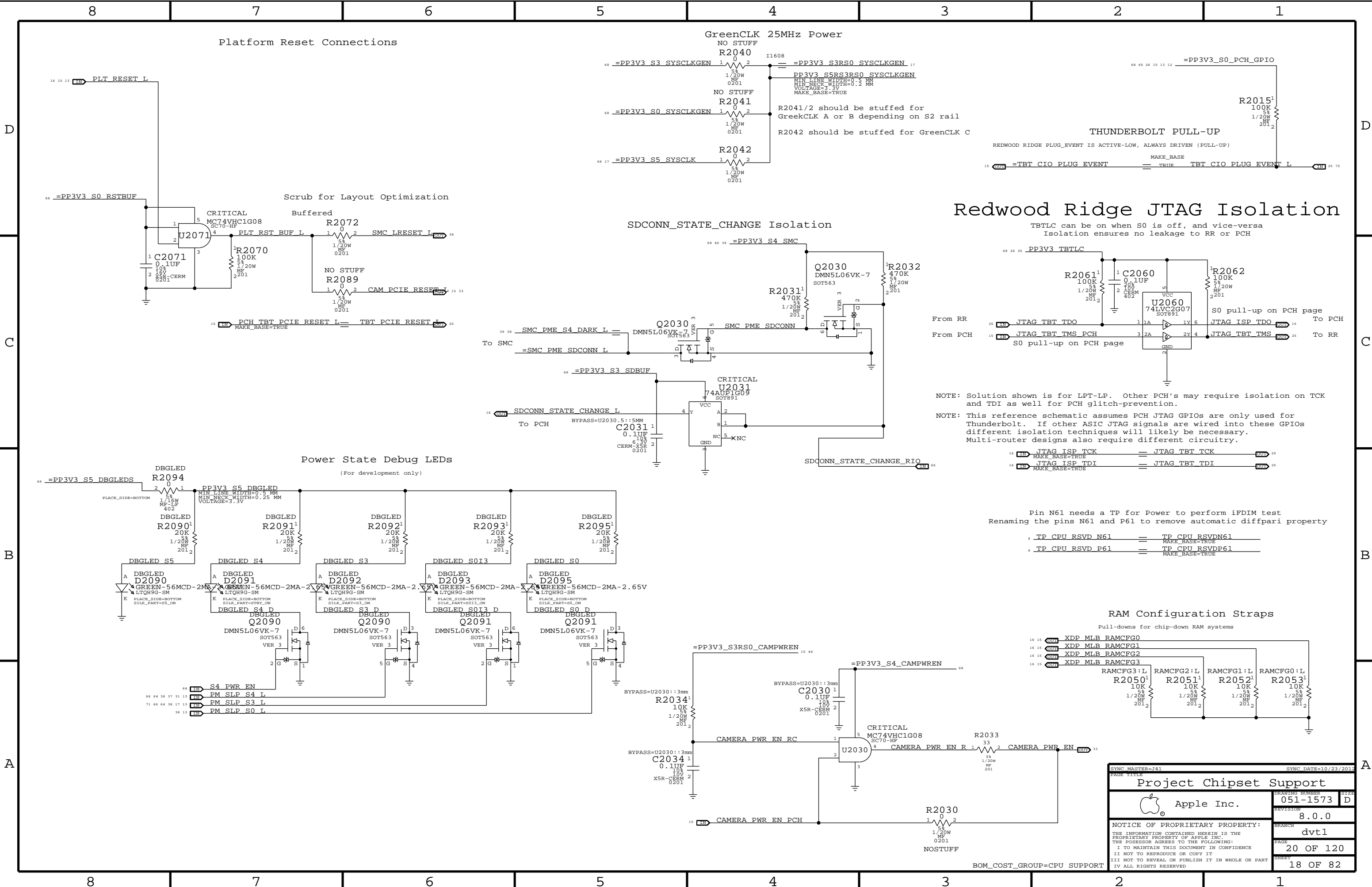
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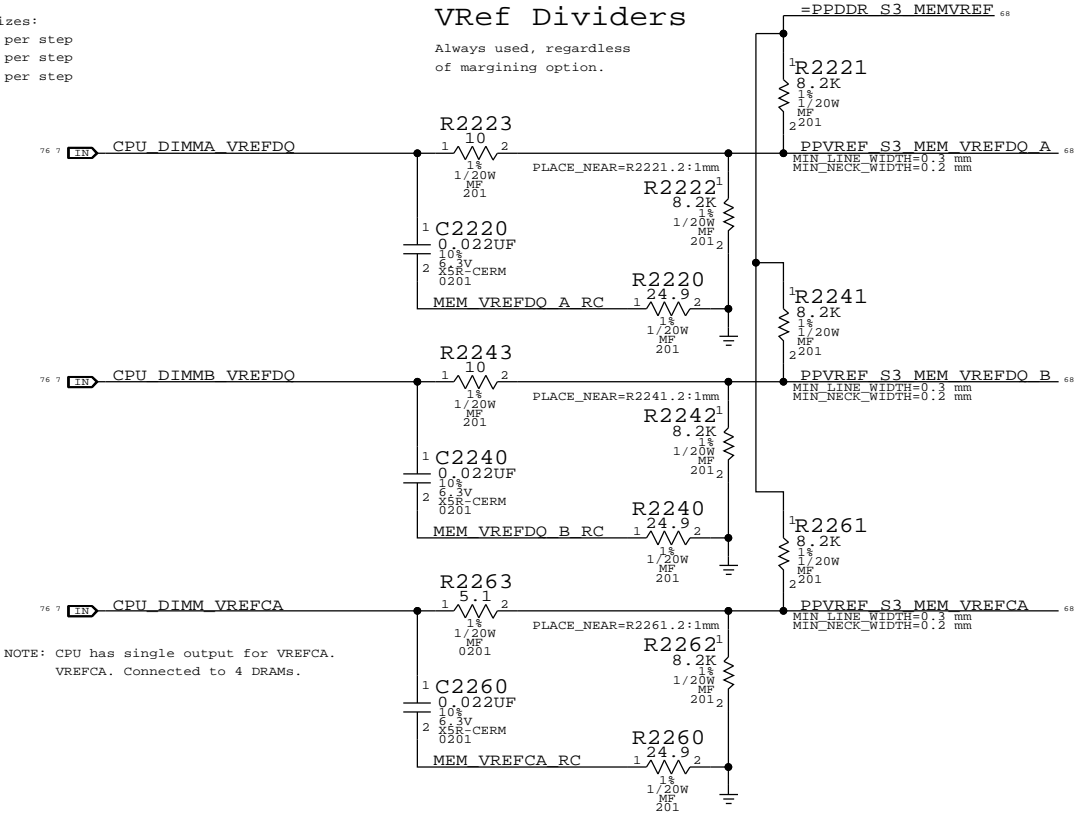
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CPU-Based Margining

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ??mV per step



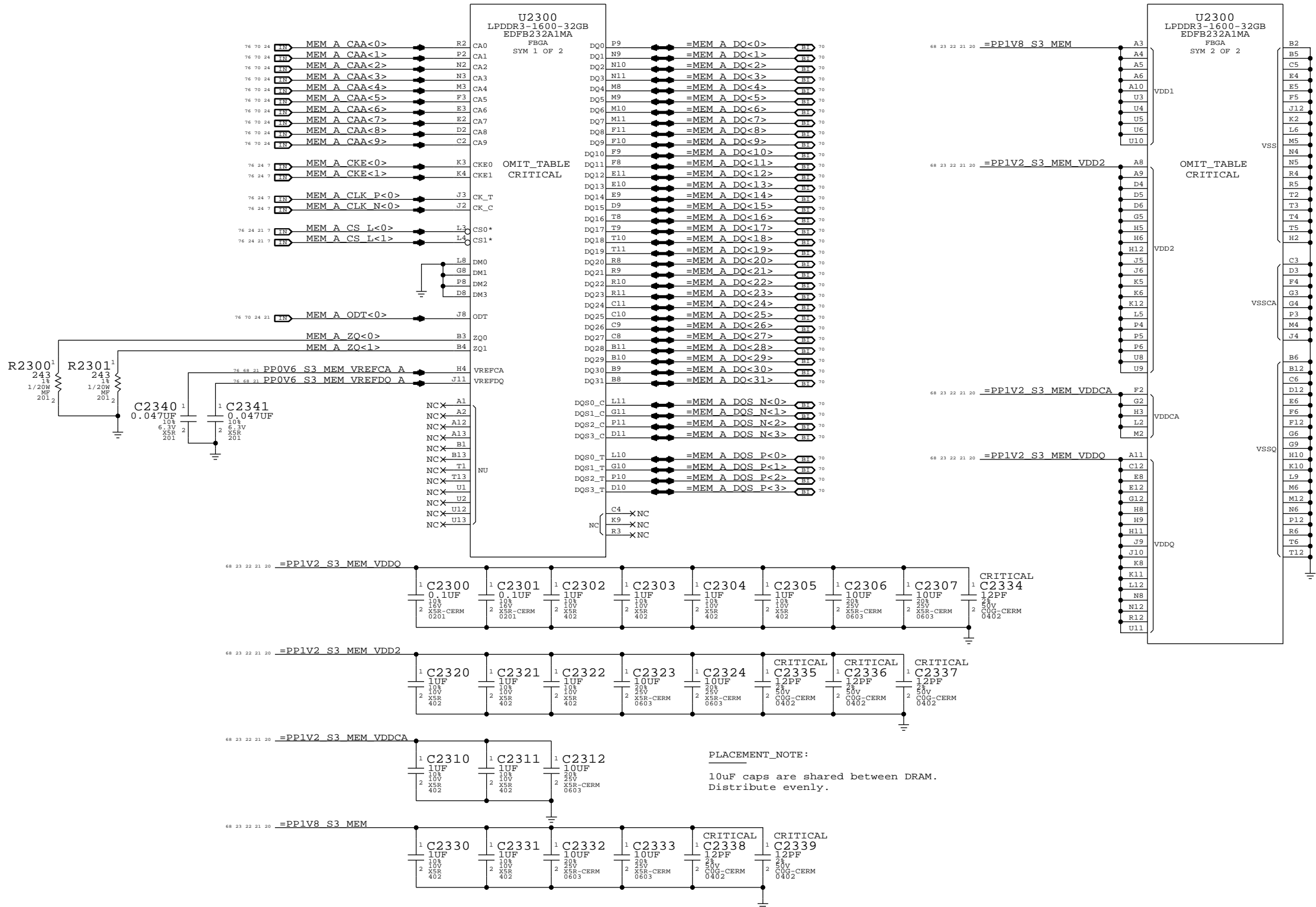
	MEM A VREF DQ		MEM B VREF DQ		MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A		B		C	C	D	
PCA9557D Pin:	1		2		3	4	5	
	LPDDR3 (1.2V)				DDR3L (1.35V)			
Nominal value	0.600V (DAC: 0x2E.5)				0.675V (DAC: 0x34)		1.200V (DAC: 0x5D)	
Margined target:	0.300V - 0.900V (+/- 300mV)				0.337V - 1.013V (+/- 337.5mV)		0.800V - 1.600V (+/- 400mV)	
DAC range:	0.000V - 1.199V (0x00 - 0x5D)				0.000V - 1.354V (0x00 - 0x69)		0.000V - 2.397V (0x00 - 0xBA)	
VRef current:	+73uA - -73uA (- = sourced)				+82uA - -82uA (- = sourced)		+21uA - -21uA (- = sourced)	
DAC step size:	6.36mV / step @ output				6.36mV / step @ output		4.28mV / step @ output	


NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

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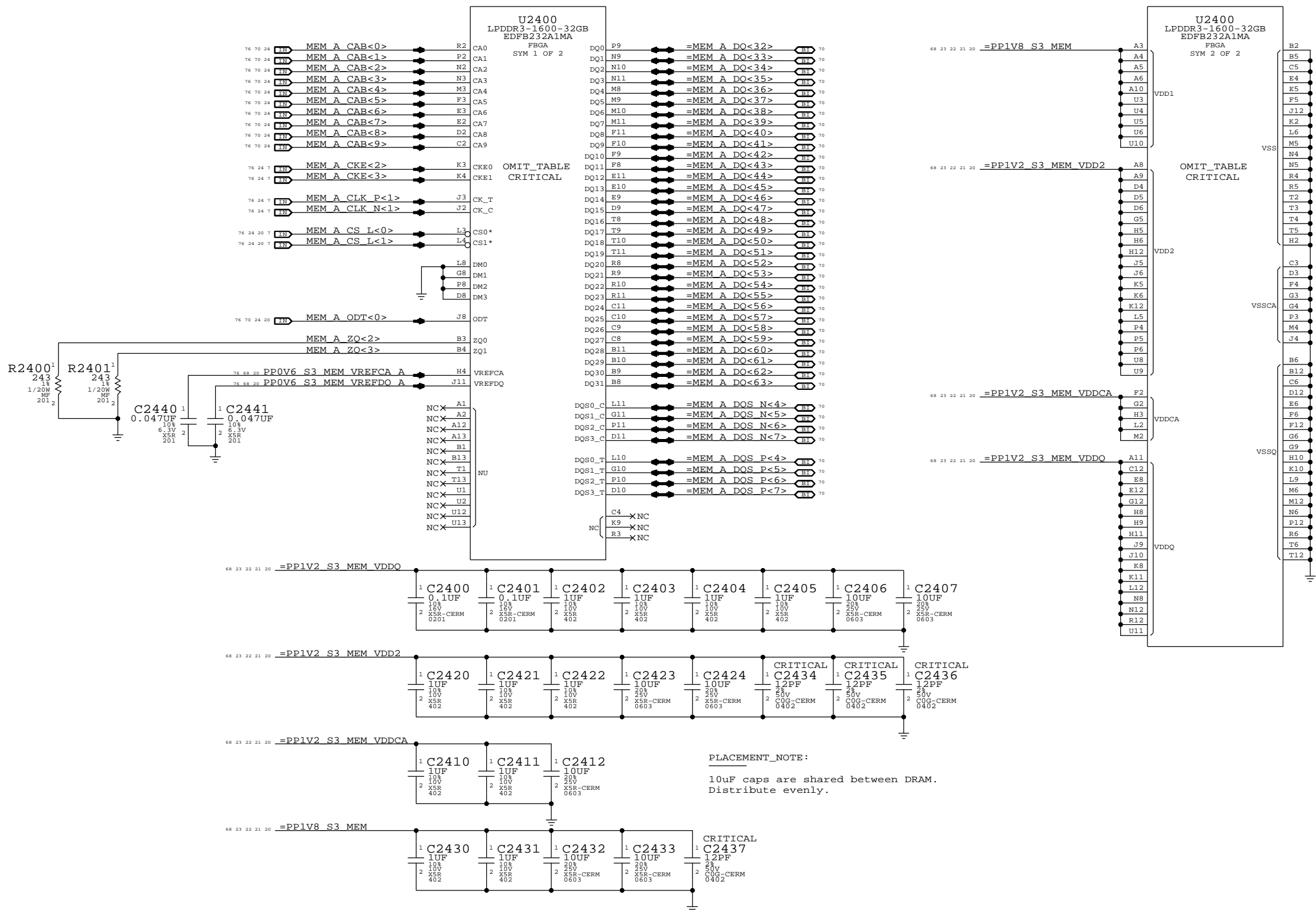
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LPDDR3 CHANNEL A (0-31)



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LPDDR3 CHANNEL A (32-63)

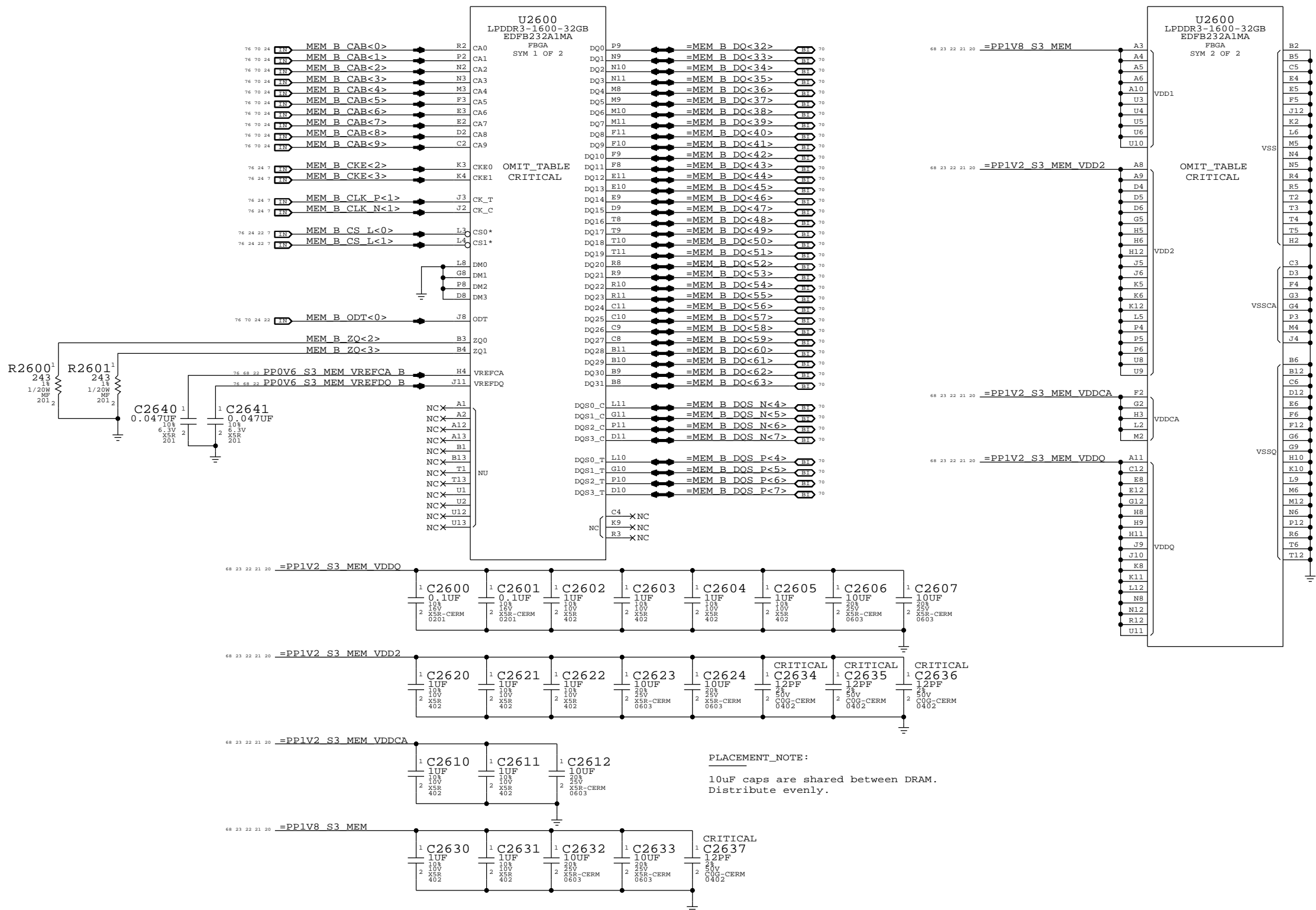



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LPDDR3 CHANNEL B (32-63)



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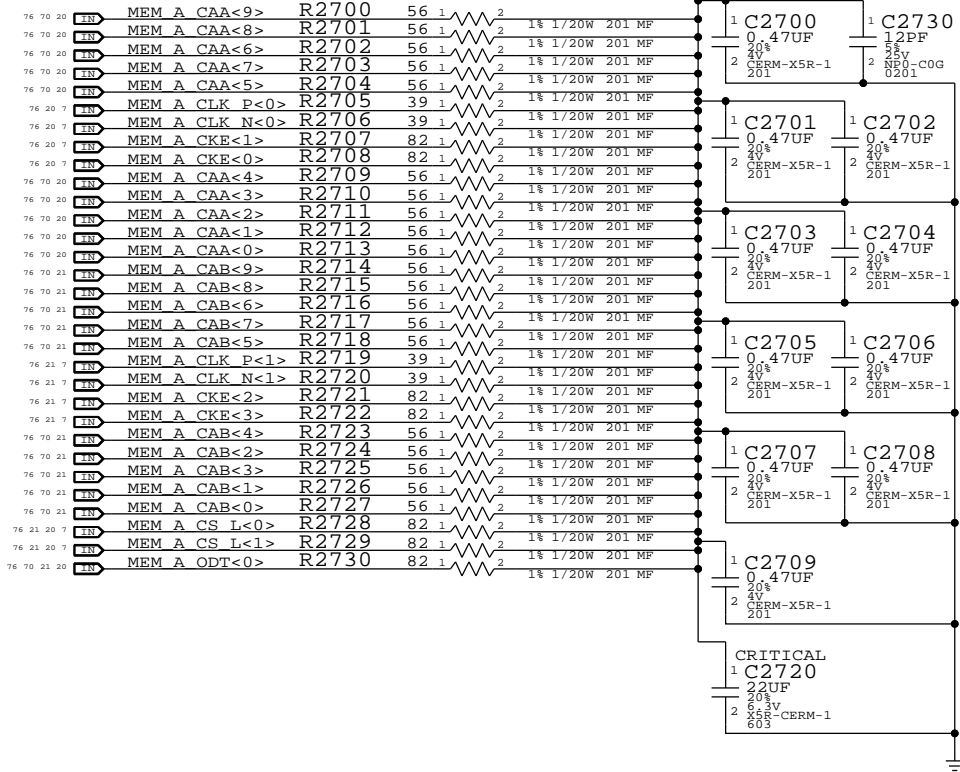
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Intel recommends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK

==PPOV6_S0_MEM_VTT_A



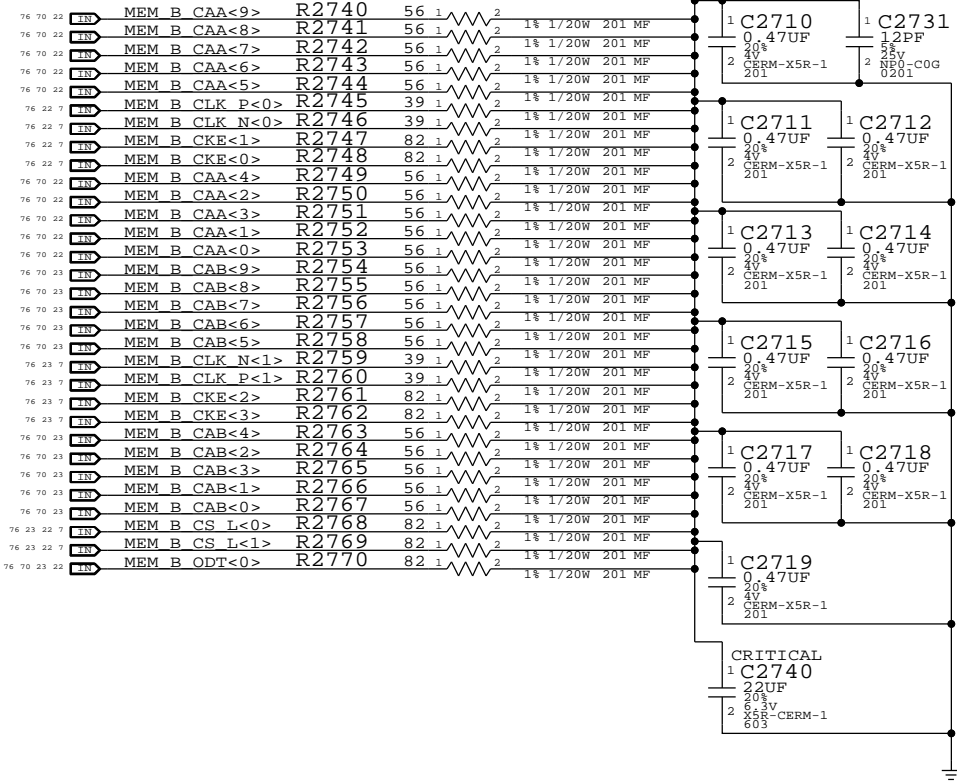
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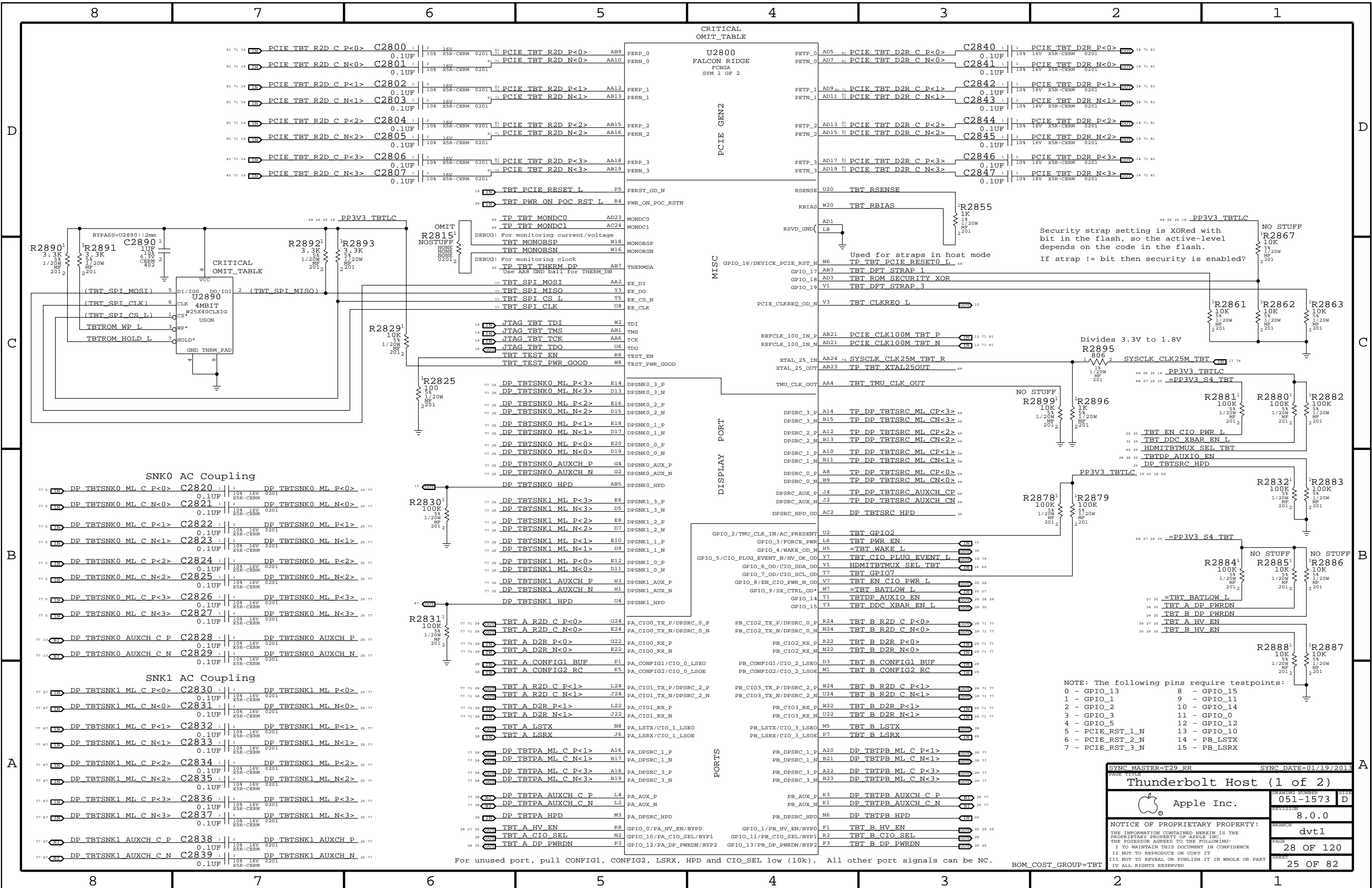
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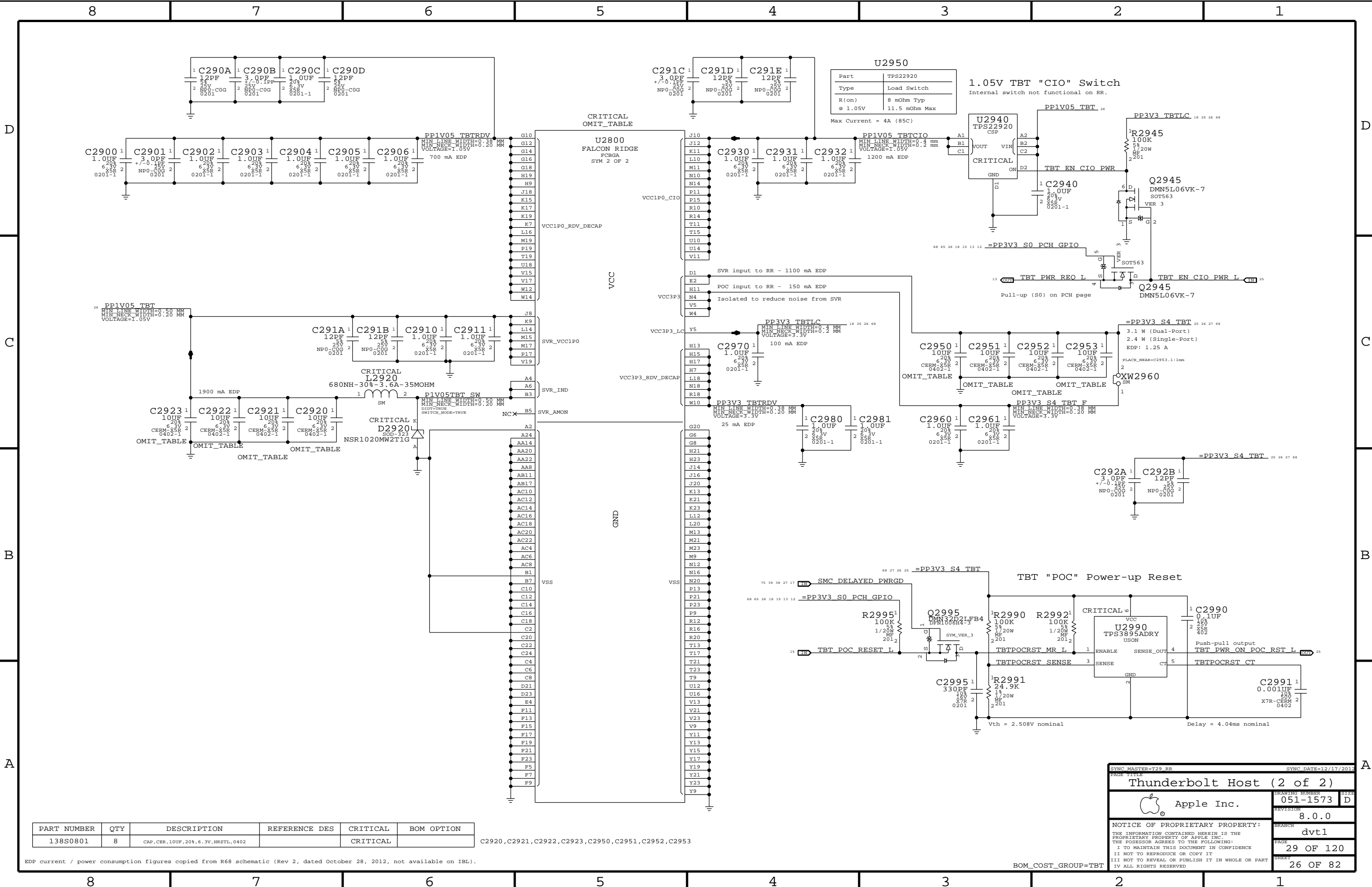
==PPOV6_S0_MEM_VTT_B



SYNC_MASTER=J41_MLB		SYNC_DATE=02/06/2013	
PAGE TITLE			
LPDDR3 DRAM Termination			
 Apple Inc.	DRAWING NUMBER	051-1573	SIZE D
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		PAGE	27 OF 120
		SHEET	24 OF 82

BOM_COST_GROUP=DRAM





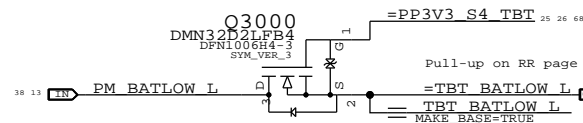
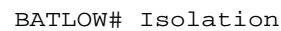
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0801	8	CAP,CER,10UF,20%,6.3V,HRZTL,0402		CRITICAL	


C2920,C2921,C2922,C2923,C2950,C2951,C2952,C2953

PAGE TITLE		PAGE NUMBER	
Thunderbolt Host (2 of 2)		051-1573	
Apple Inc.		REVISION	
		8.0.0	
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EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

BOM_COST_GROUP=TBT



SYNC MASTER=T29 RR		SYNC DATE=11/19/2015	
PAGE TITLE			
Thunderbolt Mobile Support			
 Apple Inc.	DRAWING NUMBER	051-1573	
	SIZE	D	
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	BRANCH	dvt1	
	PAGE	30 OF 120	
	SHEET	27 OF 82	





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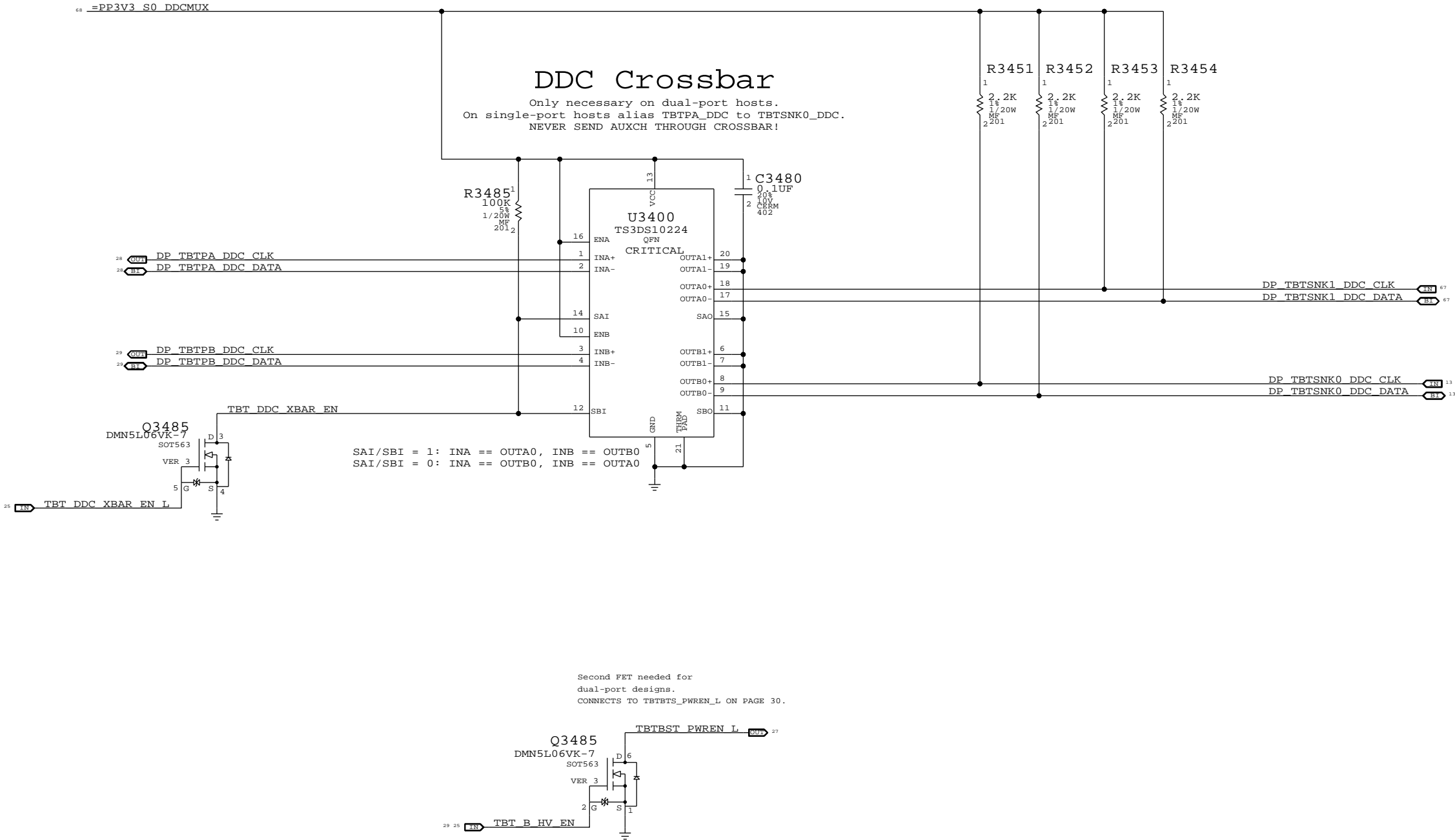
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DDC Pull-Ups

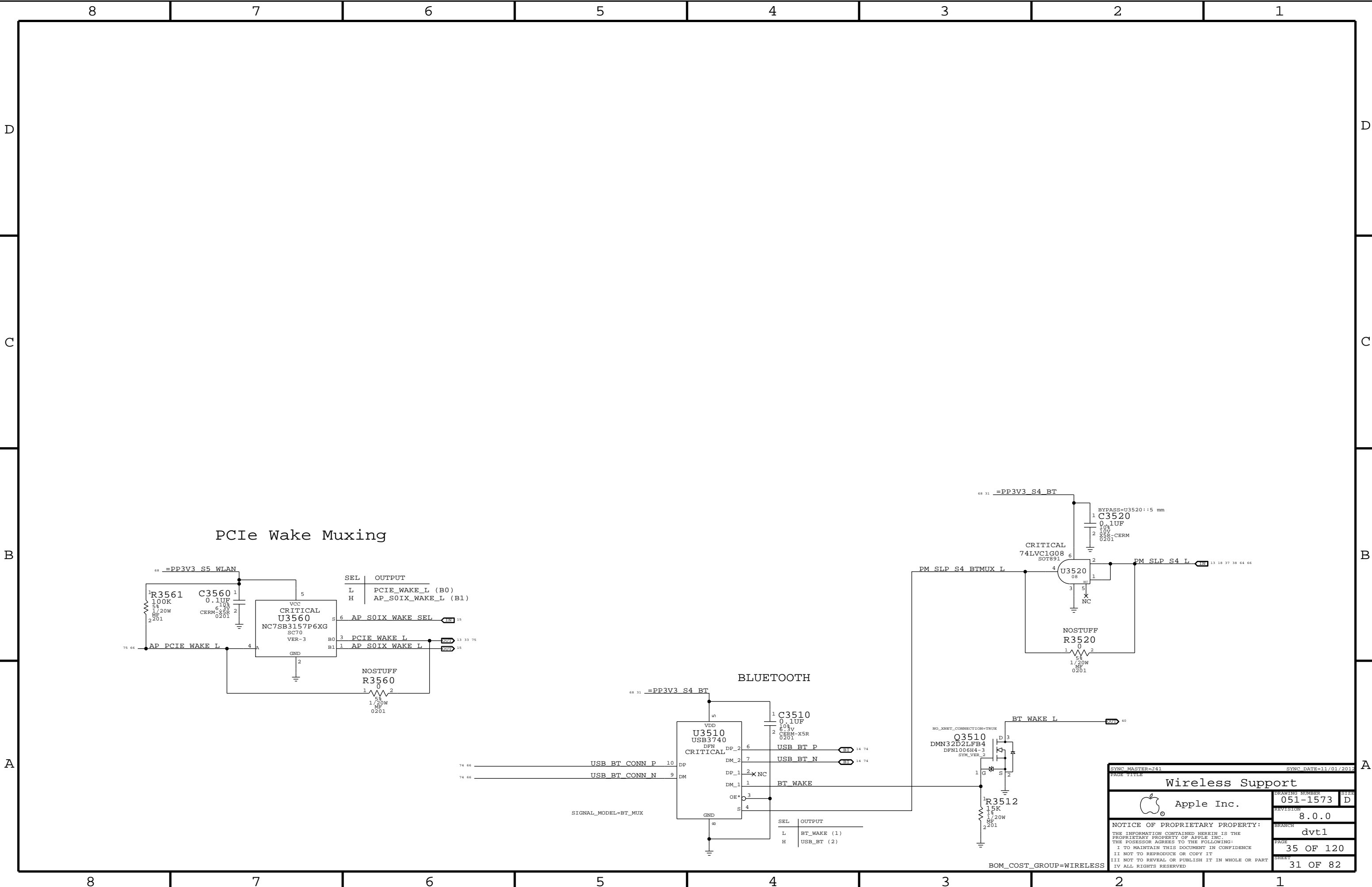
2.2k pull-ups are required by PCH to indicate active display interface.
DP++ spec violation, should remove!

NOTE: Only DDC_DATA is sensed, so DDC_CLK pull-ups are unstuffed.



SYNC MASTER=J14		SYNC DATE=10/23/2012	
PAGE TITLE			
DDC Crossbar			
 Apple Inc.	DRAWING NUMBER	051-1573	SIZE D
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BOM_COST_GROUP=TBT



SYNC MASTER=J41

SYNC DATE=11/01/2012

Wireless Support

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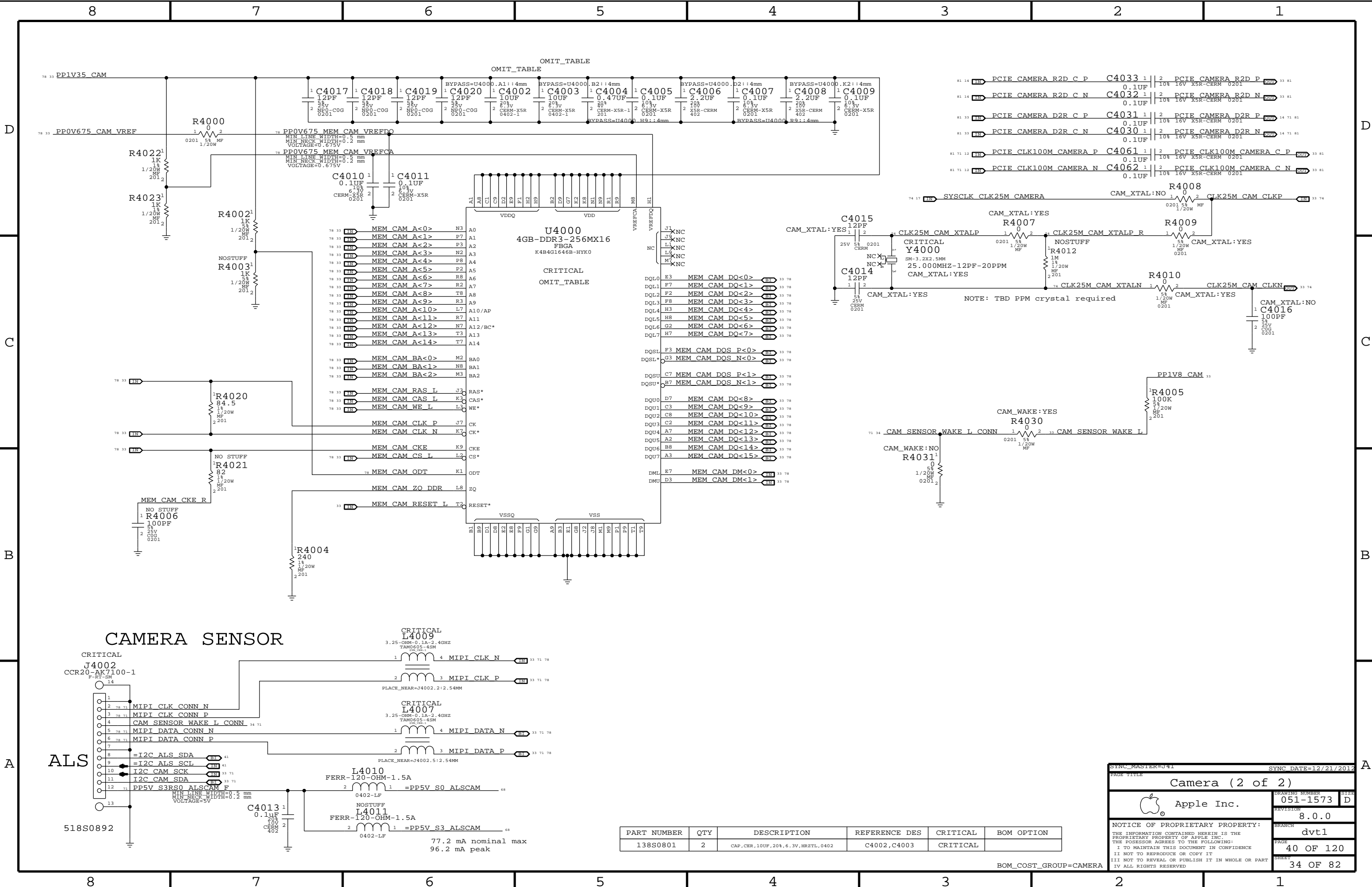
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SHEET

31 OF 82

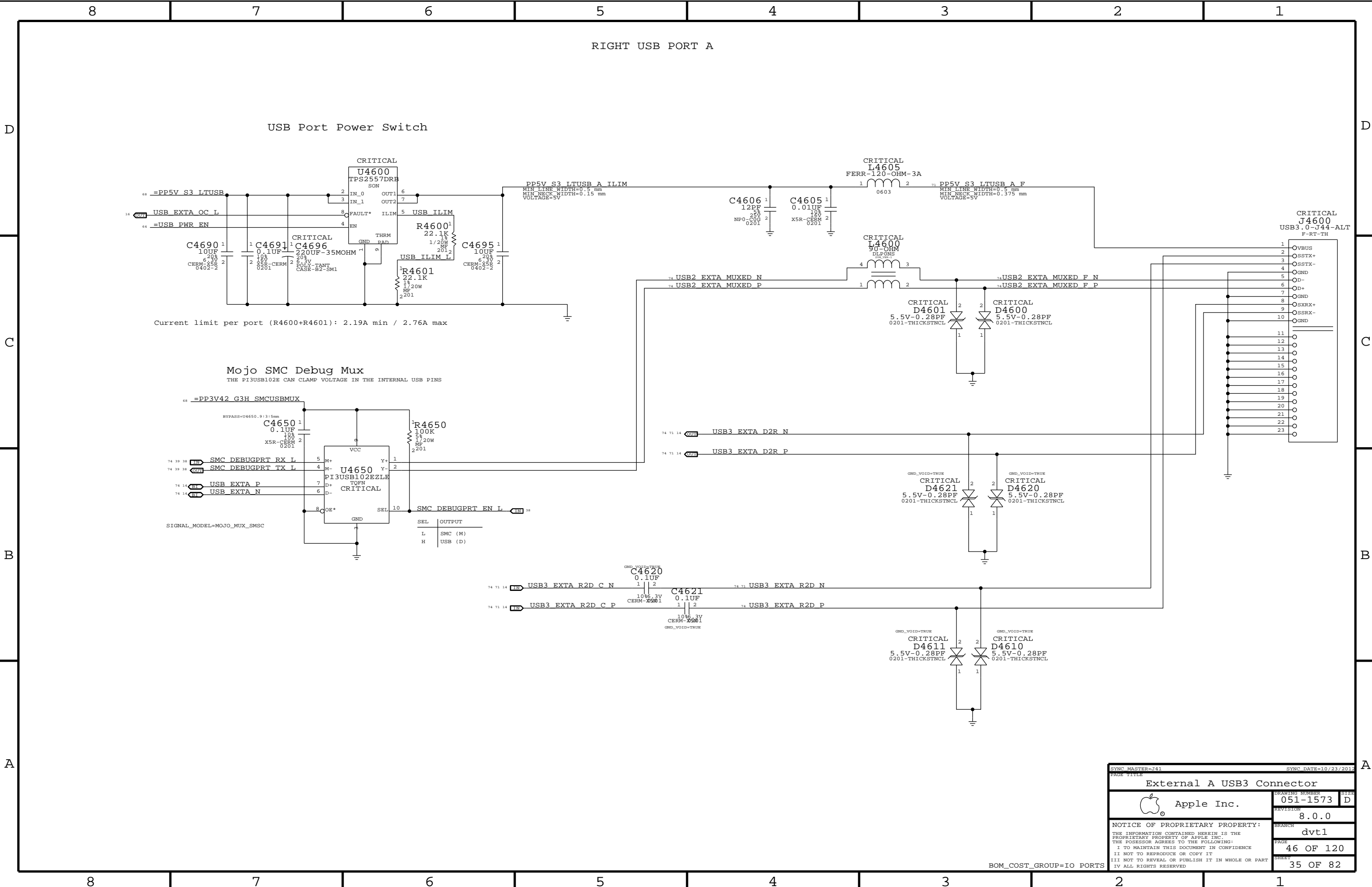
BOM_COST_GROUP=WIRELESS






PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0801	2	CAP,CER,10UF,20%,6.3V,HRZTL,0402	C4002,C4003	CRITICAL	

Camera (2 of 2)		DRAWING NUMBER	051-1573	SIZE	D
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SYNC MASTER=J41		SYNC DATE=10/23/2012	
PAGE TITLE			
External A USB3 Connector			
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		SHEET	35 OF 82



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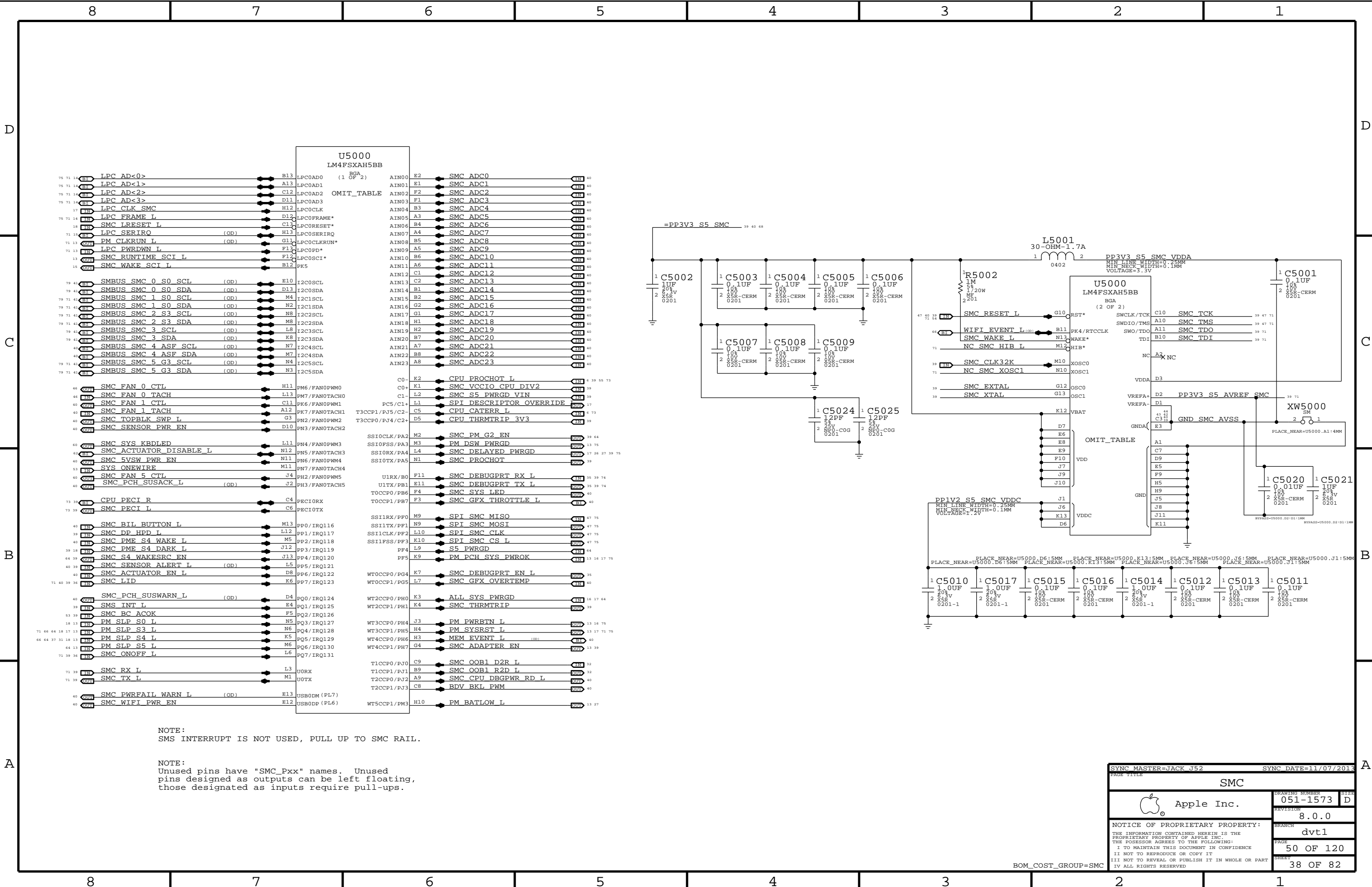


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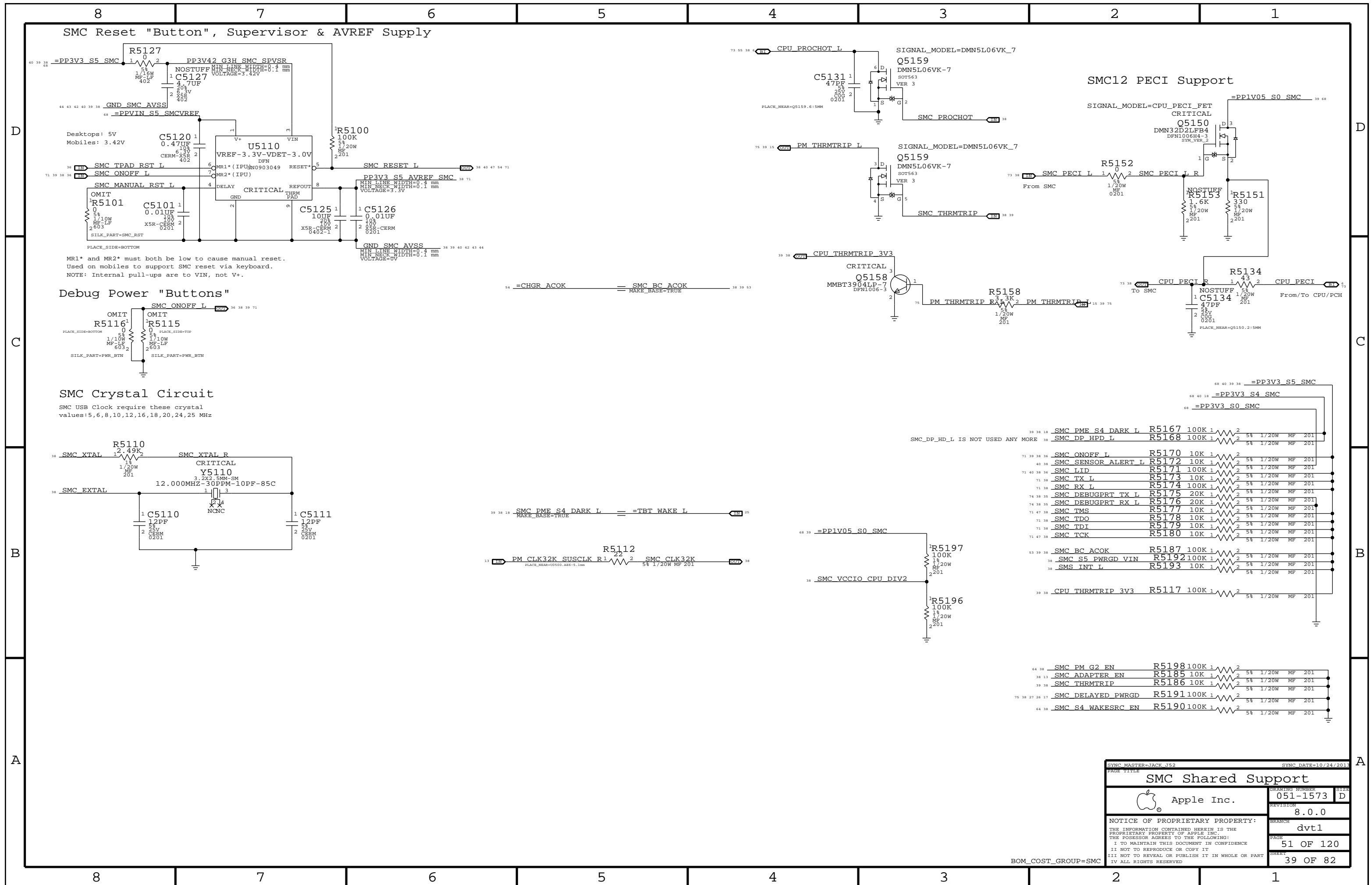


NOTE:
SMS INTERRUPT IS NOT USED, PULL UP TO SMC RAIL.

NOTE:
Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

SYNC MASTER=JACK J52		SYNC DATE=11/07/2013	
PAGE TITLE			
SMC			
	Apple Inc.	DRAWING NUMBER	051-1573
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BOM_COST_GROUP=SMC



SMC12 ADC Assignments

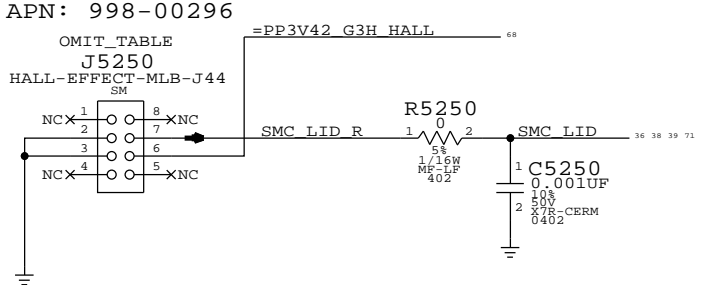
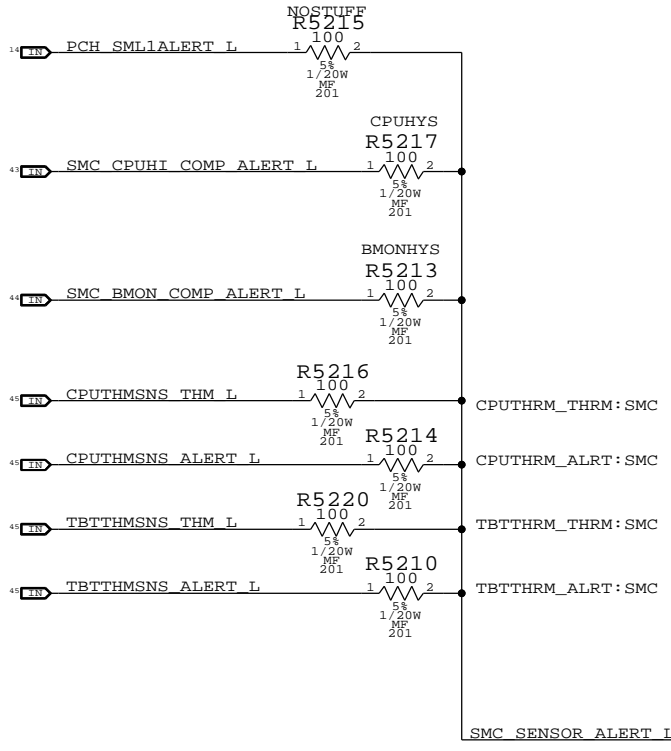
Thermal Alerts

Hall Effect Pads

D

D

38	SMC ADC0	=	SMC CPU HI ISENSE	42
38	SMC ADC1	=	SMC PBUS VSENSE	42
38	SMC ADC2	=	SMC BMON ISENSE	42
38	SMC ADC3	=	SMC DCIN ISENSE	42
38	SMC ADC4	=	SMC DCIN VSENSE	42
38	SMC ADC5	=	SMC BMON DISCRETE ISENSE	42
38	SMC ADC6	=	SMC CPU ISENSE	43
38	SMC ADC7	=	SMC OTHER5V HI ISENSE	42
38	SMC ADC8	=	SMC OTHER3V3 HI ISENSE	42
38	SMC ADC9	=	SMC DDR ISENSE	43
38	SMC ADC10	=	SMC LCDBKLT ISENSE	42
38	SMC ADC11	=	SMC TPAD ISENSE	42
38	SMC ADC12	=	SMC DDR1V8 ISENSE	43
38	SMC ADC13	=	SMC SSD ISENSE	43
38	SMC ADC14	=	SMC PP3V3S0 ISENSE	43
38	SMC ADC15	=	SMC CAMERA ISENSE	44
38	SMC ADC16	=	SMC TPAD VSENSE	42
38	SMC ADC17	=	SMC PP5VS0 ISENSE	42
38	SMC ADC18	=	SMC CPUDDR ISENSE	43
38	SMC ADC19	=	SMC PCH ISENSE	43
38	SMC ADC20	=	SMC CPU VSENSE	44
38	SMC ADC21	=	SMC LCDPANEL ISENSE	44
38	SMC ADC22	=	SMC CPU IMON ISENSE	44
38	SMC ADC23	=	SMC TBT ISENSE	44



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-01216	1	SUBASSY,PCBA,HALL EFFECT,X304	J5250	CRITICAL	

639-00525 (PCBA,HALL EFFECT,X304) REPORTS TO 677-01216

Specify one of these BOM GROUPS.

BOM GROUP	BOM OPTIONS
CPUTHRM:BOTH	CPUTHRM_THRM: SMC, CPUTHRM_ALRT: SMC
CPUTHRM:THRM	CPUTHRM_THRM: SMC, CPUTHRM_ALRT: PU
CPUTHRM:ALRT	CPUTHRM_THRM: PU, CPUTHRM_ALRT: SMC
CPUTHRM:NONE	CPUTHRM_THRM: PU, CPUTHRM_ALRT: PU

Specify one of these BOM GROUPS.

BOM GROUP	BOM OPTIONS
TBTTHRM:BOTH	TBTTHRM_THRM: SMC, TBTTHRM_ALRT: SMC
TBTTHRM:THRM	TBTTHRM_THRM: SMC, TBTTHRM_ALRT: PU
TBTTHRM:ALRT	TBTTHRM_THRM: PU, TBTTHRM_ALRT: SMC
TBTTHRM:NONE	TBTTHRM_THRM: PU, TBTTHRM_ALRT: PU

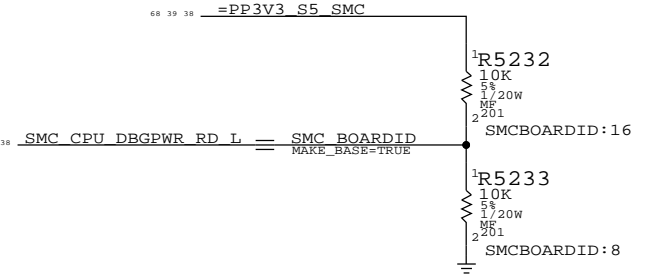
Requires EMC1412-1 or EMC1412-2 instead of EMC1412-A, new APN needs to be created.

C

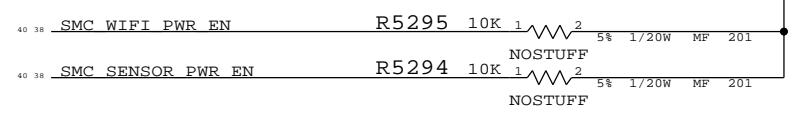
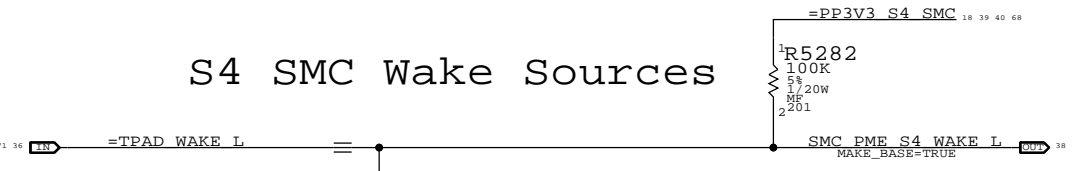
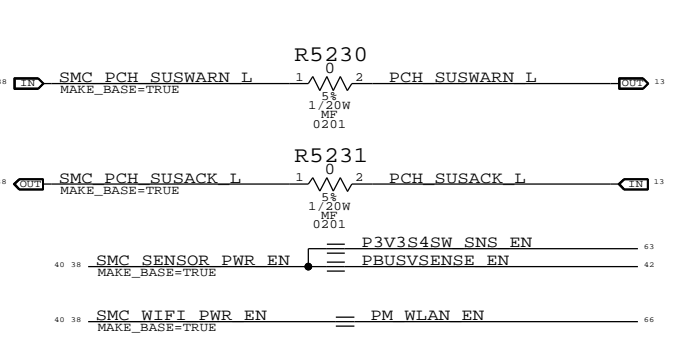
C

SMC12 Pin Assignments

38	SMBUS SMC 4 ASF SCL	=	NC SMBUS SMC 4 ASF SCL	
38	SMBUS SMC 4 ASF SDA	=	NC SMBUS SMC 4 ASF SDA	
38	BDV BKL PWM	=	NC SMC TPAD BOOST DISABLE L	
38	SMC SYS LED	=	NC SMC SYS LED	
38	SMC GFX THROTTLE L	=	NC SMC GFX THROTTLE L	
38	SMC GFX OVERTEMP	=	NC SMC GFX OVERTEMP	
38	SMC FAN 1 CTL	=	NC SMC FAN 1 CTL	
38	SMC FAN 1 TACH	=	NC SMC FAN 1 TACH	
38	SMC 5VSW PWR EN	=	NC SMC 5VSW PWR EN	
38	SMC FAN 5 CTL	=	NC SMC FAN 5 CTL	
38	SMC BIL BUTTON L	=	NC SMC BIL BUTTON L	
38	MEM EVENT L	=	NC MEM EVENT L	
38	SMC PWRFAIL WARN L	=	NC SMC PWRFAIL WARN L	



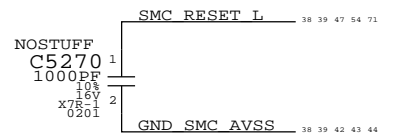
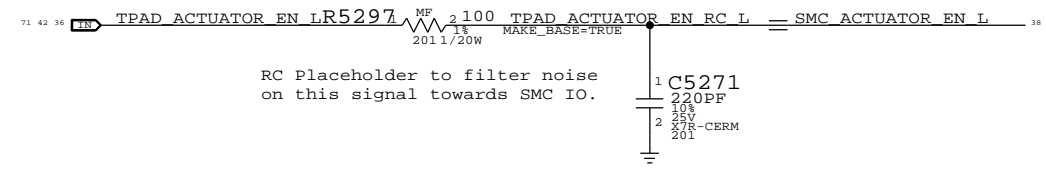
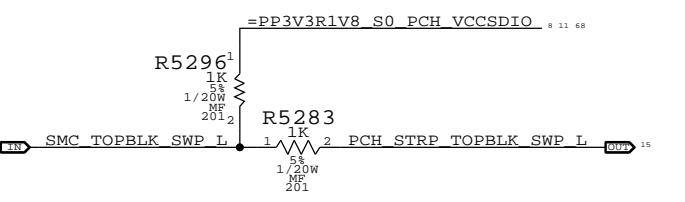
S4 SMC Wake Sources



B

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Top Block Swap



SMC Project Support

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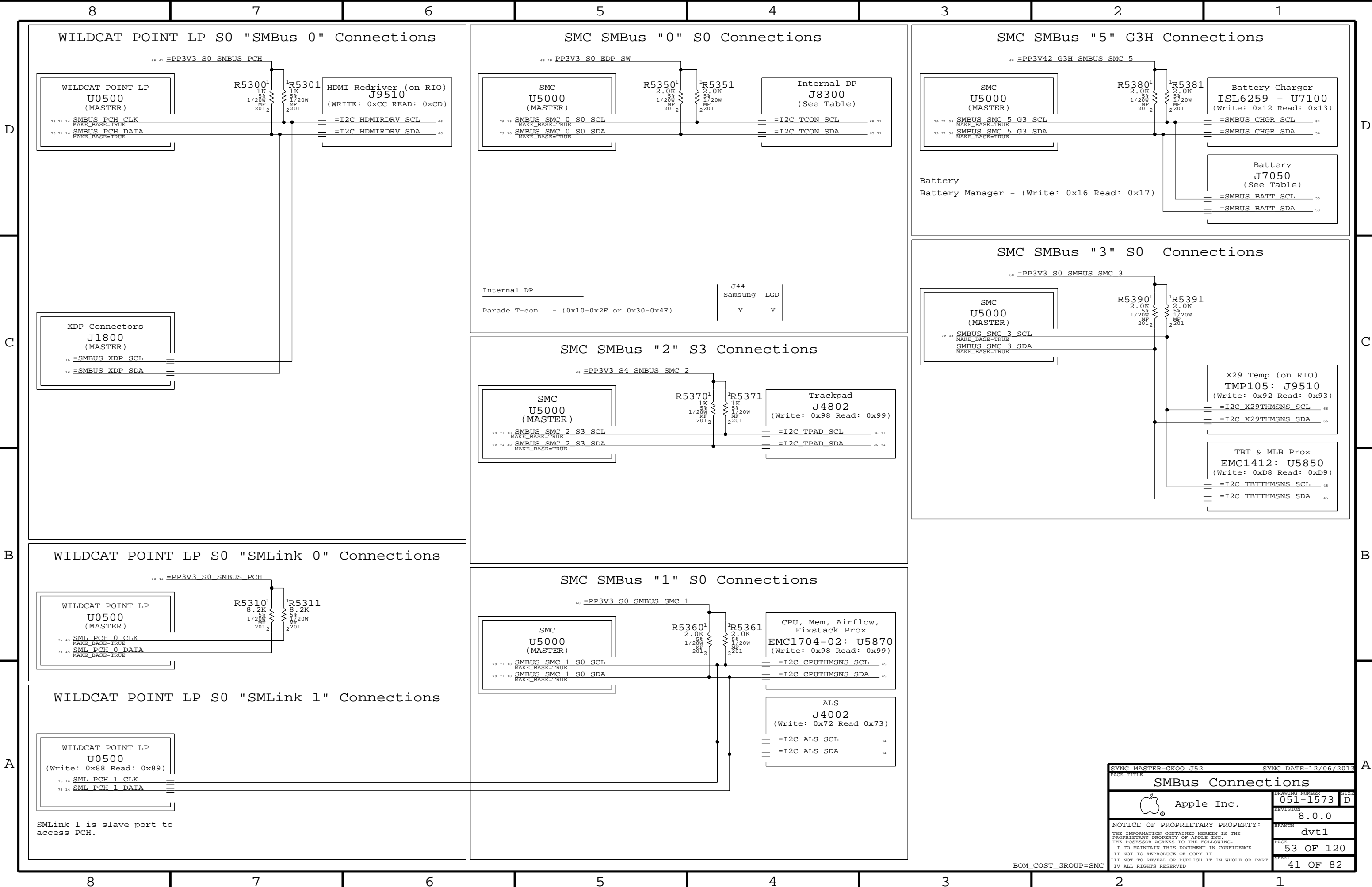
SIZE

D

BOM_COST_GROUP=SMC

A


A



SYNC MASTER=GKOO J52

SYNC DATE=12/06/2013

SMBus Connections

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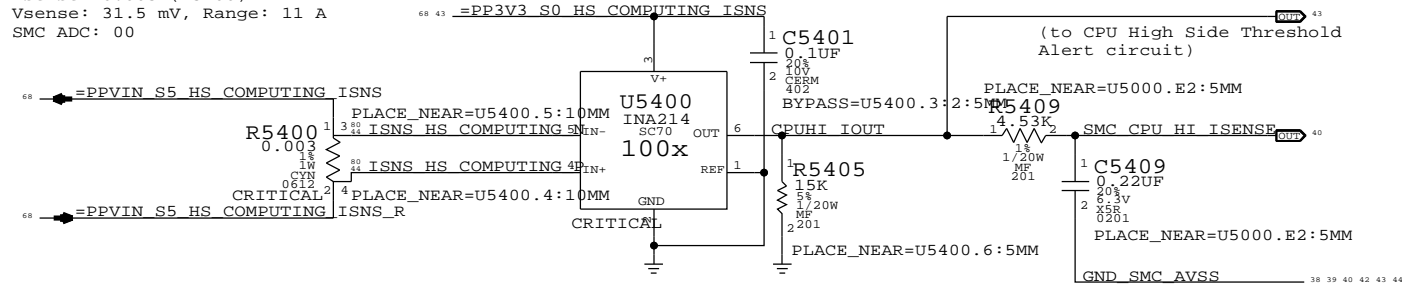
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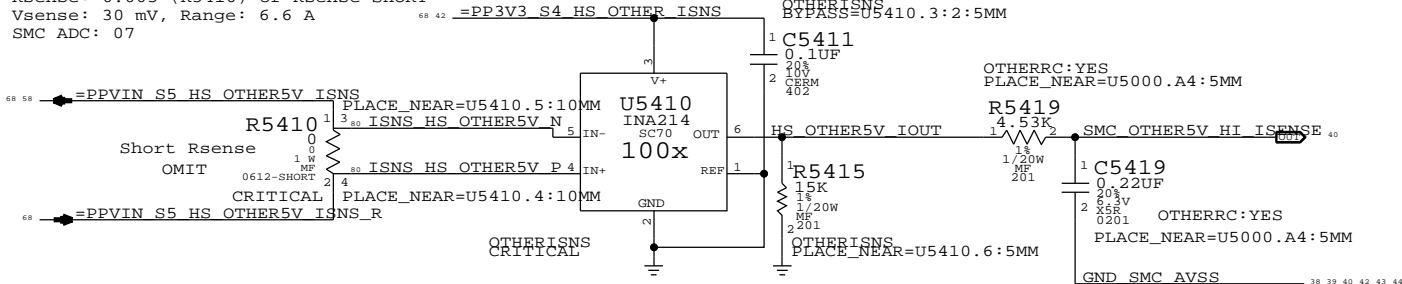
CPU High Side Current Sense (IC0R)

Gain: 100x, EDP: 10.5 A
Rsense: 0.003 (R5400)
Vsense: 31.5 mV, Range: 11 A
SMC ADC: 00



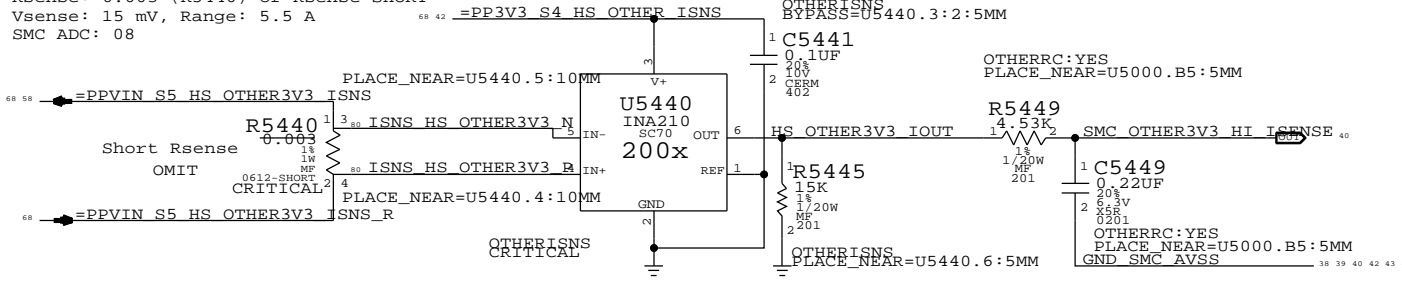
OTHER 5V High Side Current Sense (IO5R)

Gain: 100x, EDP: 6 A
Rsense: 0.005 (R5410) or Rsense SHORT
Vsense: 30 mV, Range: 6.6 A
SMC ADC: 07



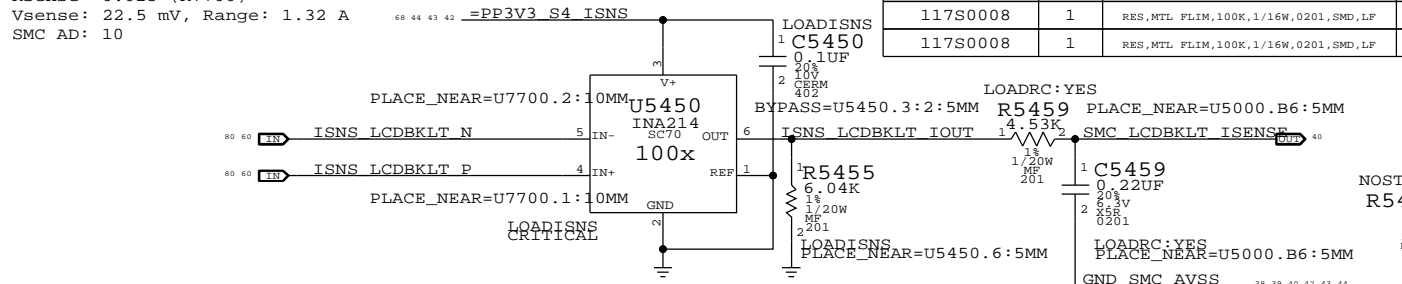
OTHER 3.3V High Side Current Sense (IO3R)

Gain: 200x, EDP: 5 A
Rsense: 0.003 (R5440) or Rsense SHORT
Vsense: 15 mV, Range: 5.5 A
SMC ADC: 08



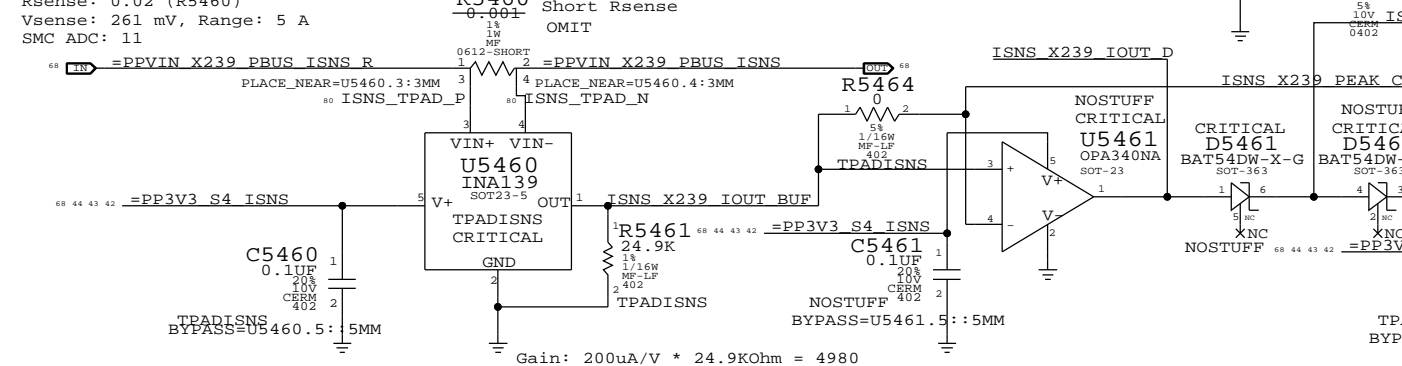
LCD Backlight Current Sense (IBLC)

Gain: 100x, EDP: 0.9 A
Rsense: 0.025 (R7700)
Vsense: 22.5 mV, Range: 1.32 A
SMC AD: 10



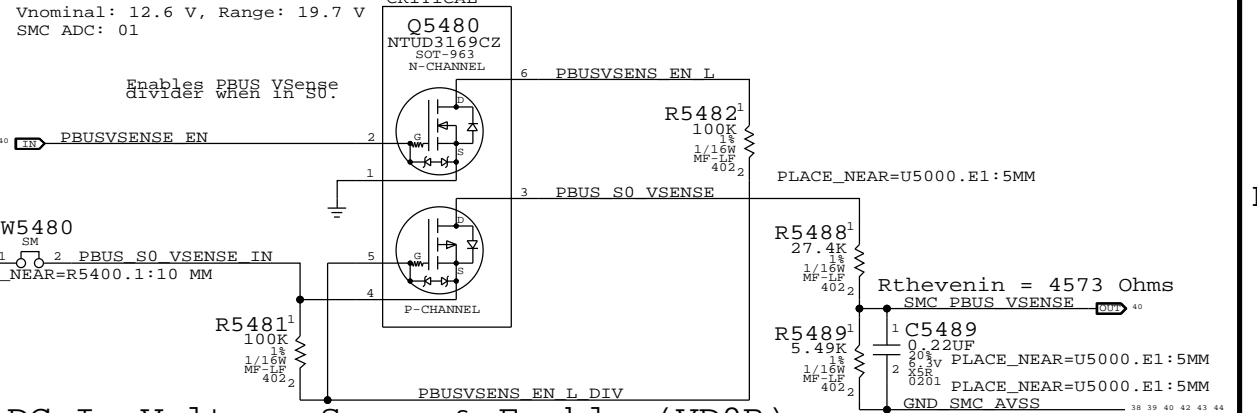
Trackpad Actuator X239 Current Sense (ITPC)

Gain: 4.99x, EDP: 2.61 A (Transient)
Rsense: 0.02 (R5460)
Vsense: 261 mV, Range: 5 A
SMC ADC: 11



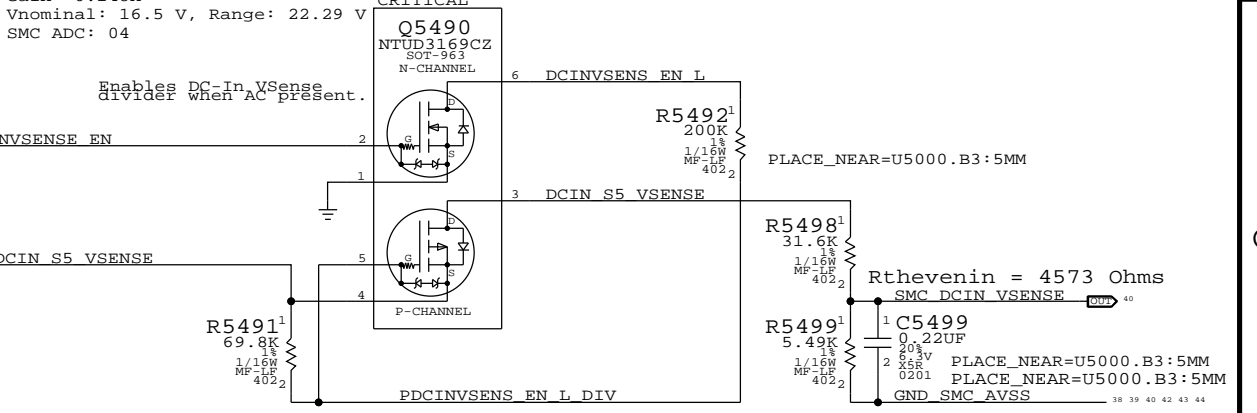
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
Vnominal: 12.6 V, Range: 19.7 V
SMC ADC: 01



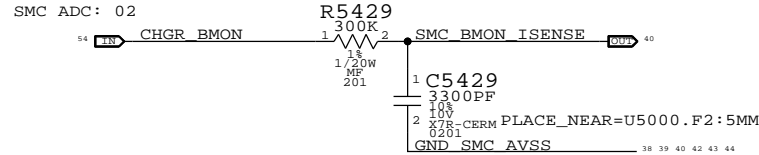
DC In Voltage Sense & Enable (VD0R)

Gain: 0.148x
Vnominal: 16.5 V, Range: 22.29 V
SMC ADC: 04



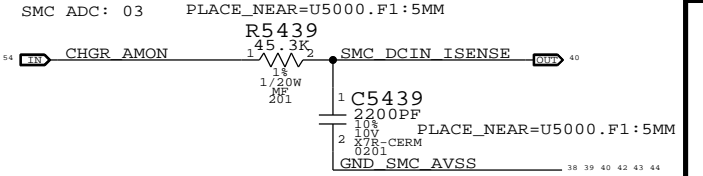
Charger (BMON) Current Sense (IPBR)

Charger Gain: 36x, EDP: 8 A
Rsense: 0.005 (R7150) PLACE_NEAR=U5000.F2:5MM
SMC ADC: 02



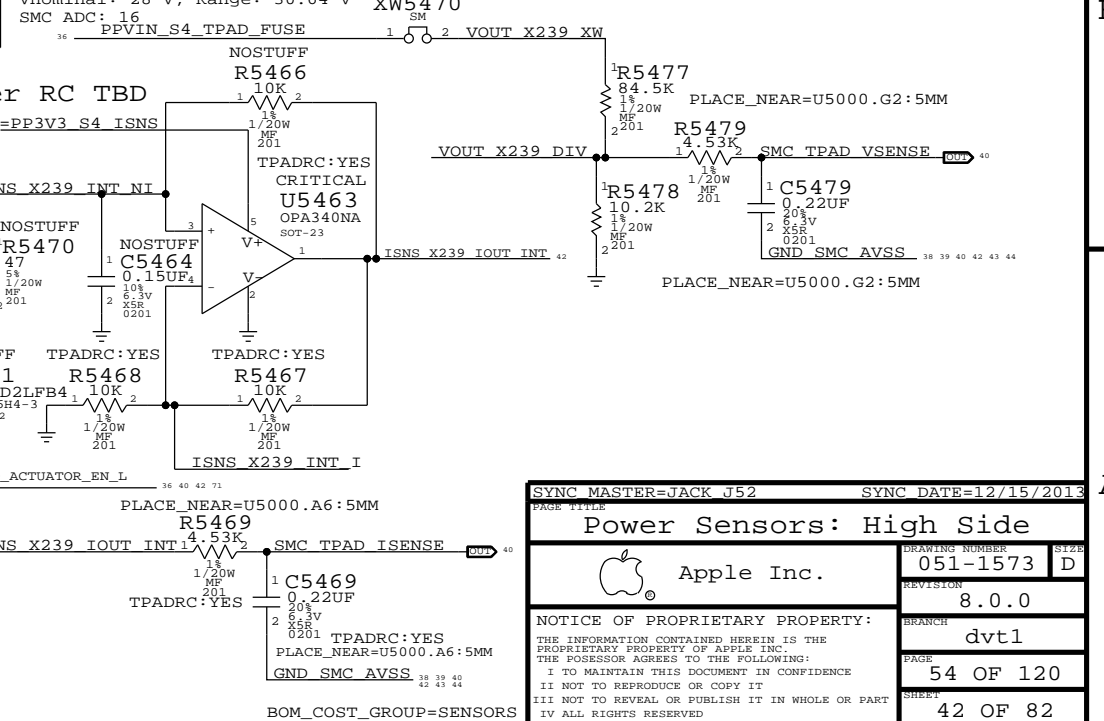
DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
Rsense: 0.020 (R7120)
SMC ADC: 03 PLACE_NEAR=U5000.F1:5MM



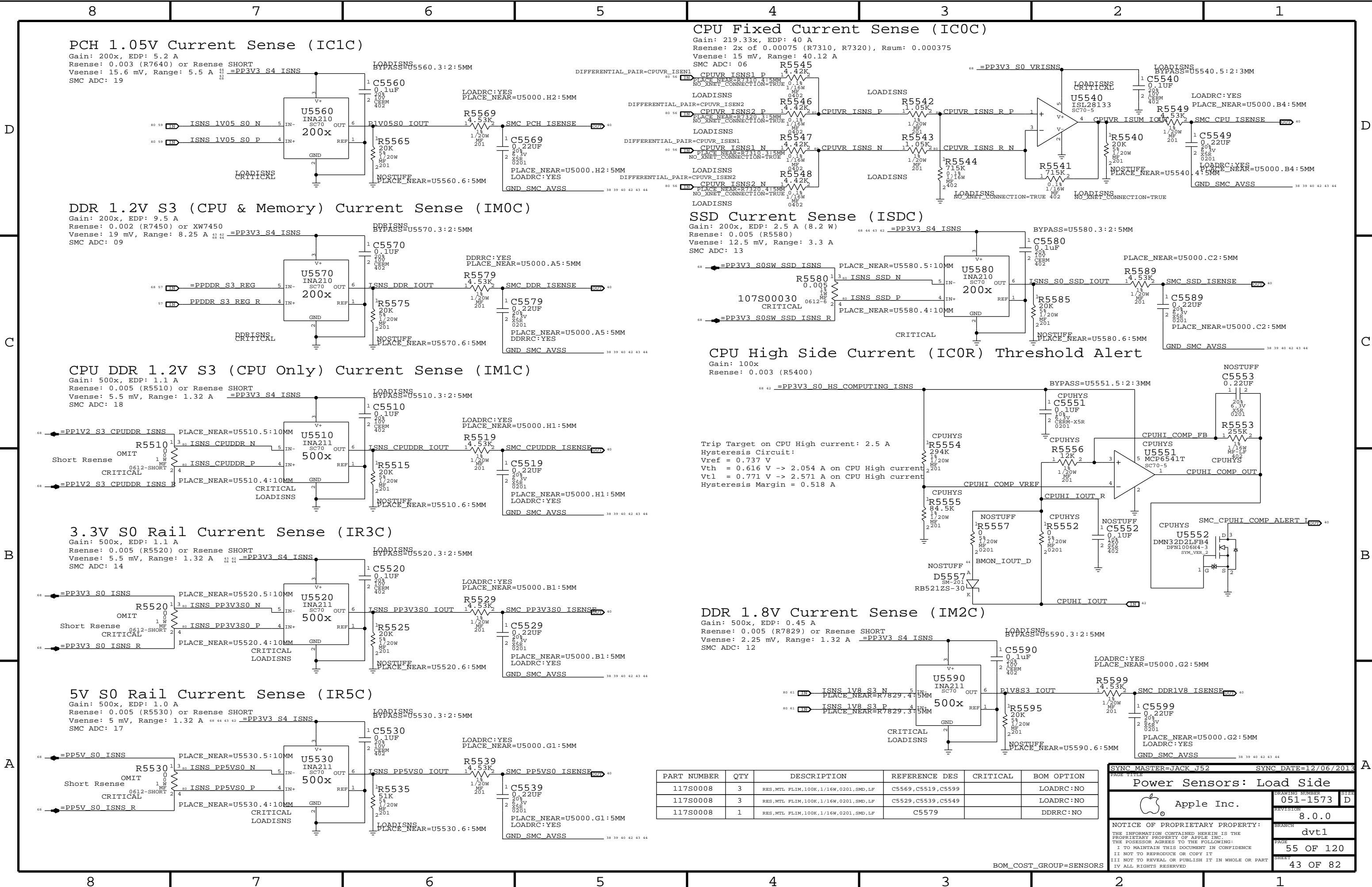
Trackpad Actuator X239 Voltage Sense (VTPC)

Gain: 0.10771
Vnominal: 28 V, Range: 30.64 V
SMC ADC: 16
PLACE_NEAR=U5000.G2:5MM



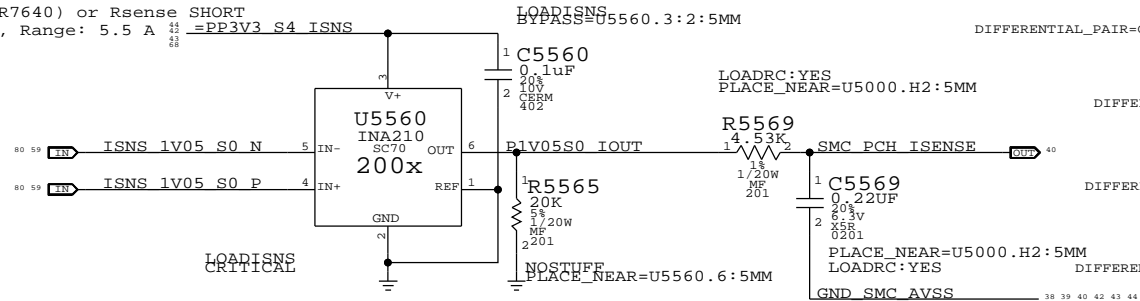
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5419,C5449		OTHERRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5459		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5469		TPADRC:NO

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Power Sensors: High Side		051-1573	
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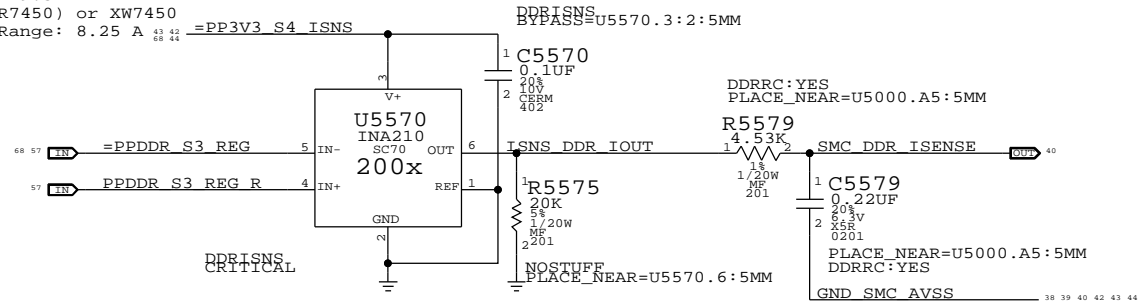
PCH 1.05V Current Sense (IC1C)

Gain: 200x, EDP: 5.2 A
Rsense: 0.003 (R7640) or Rsense SHORT
Vsense: 15.6 mV, Range: 5.5 A
SMC ADC: 19



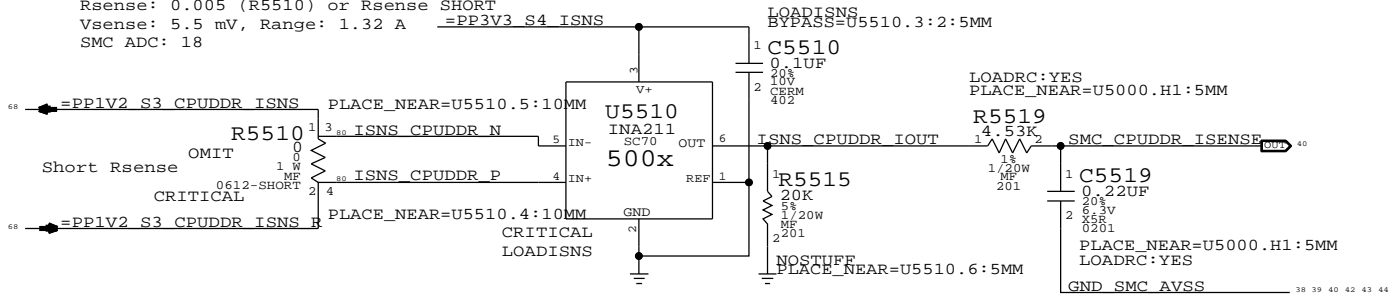
DDR 1.2V S3 (CPU & Memory) Current Sense (IM0C)

Gain: 200x, EDP: 9.5 A
Rsense: 0.002 (R7450) or XW7450
Vsense: 19 mV, Range: 8.25 A
SMC ADC: 09



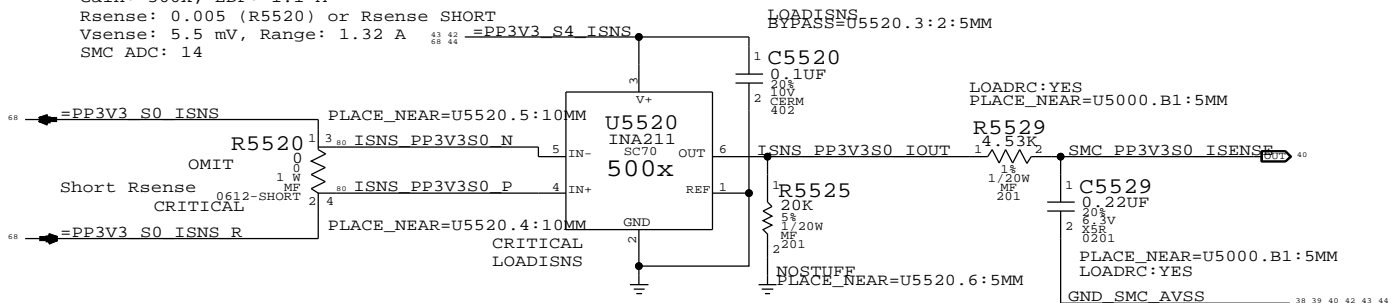
CPU DDR 1.2V S3 (CPU Only) Current Sense (IM1C)

Gain: 500x, EDP: 1.1 A
Rsense: 0.005 (R5510) or Rsense SHORT
Vsense: 5.5 mV, Range: 1.32 A
SMC ADC: 18



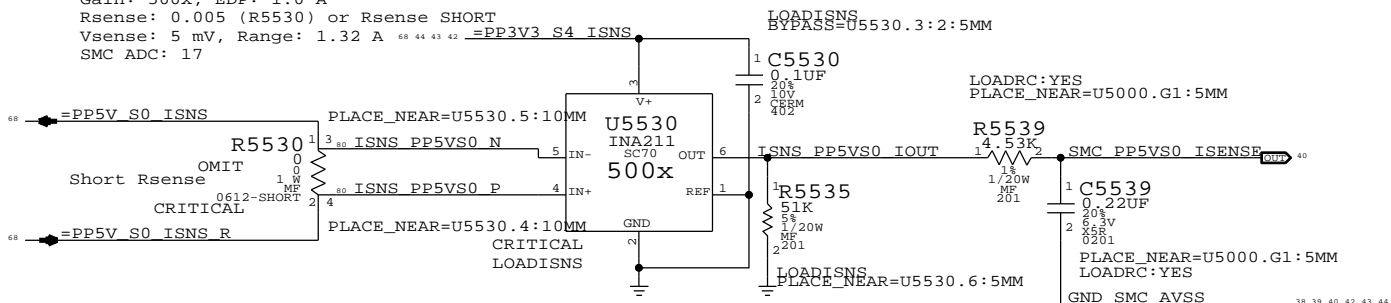
3.3V S0 Rail Current Sense (IR3C)

Gain: 500x, EDP: 1.1 A
Rsense: 0.005 (R5520) or Rsense SHORT
Vsense: 5.5 mV, Range: 1.32 A
SMC ADC: 14



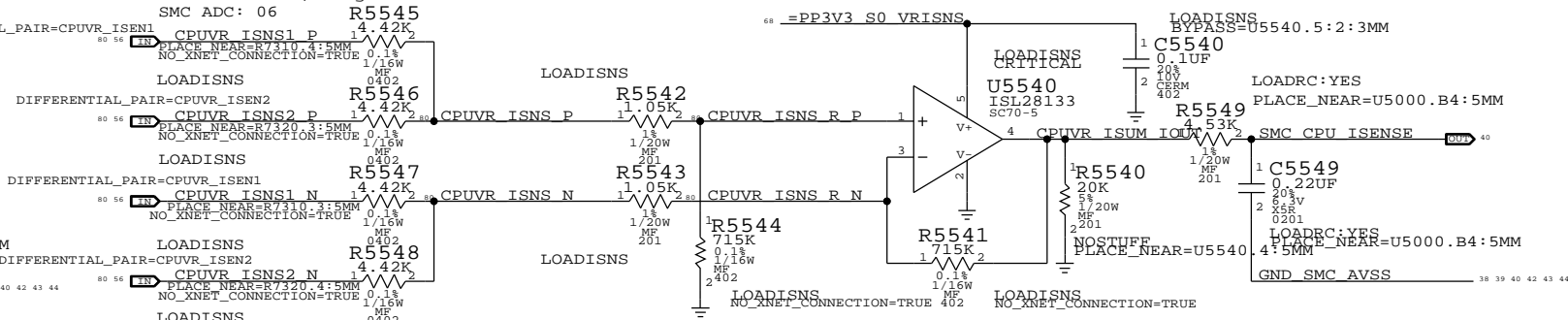
5V S0 Rail Current Sense (IR5C)

Gain: 500x, EDP: 1.0 A
Rsense: 0.005 (R5530) or Rsense SHORT
Vsense: 5 mV, Range: 1.32 A
SMC ADC: 17



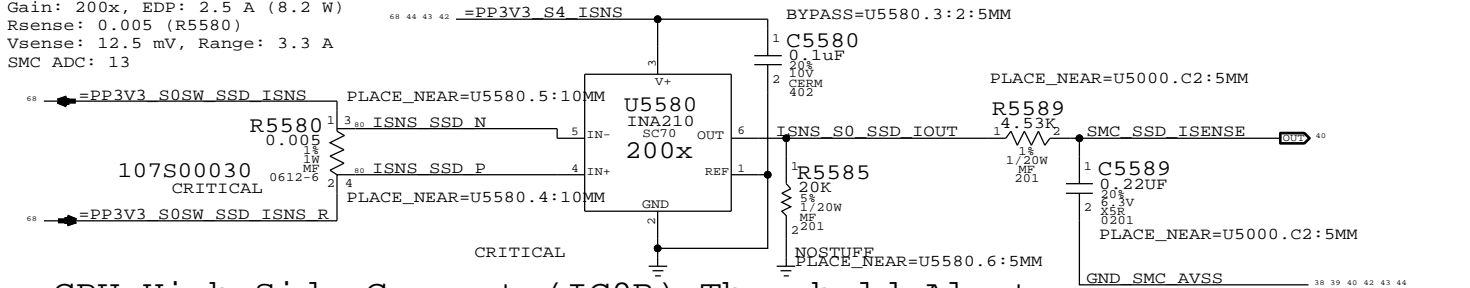
CPU Fixed Current Sense (IC0C)

Gain: 219.33x, EDP: 40 A
Rsense: 2x of 0.00075 (R7310, R7320), Rsum: 0.000375
Vsense: 15 mV, Range: 40.12 A
SMC ADC: 06



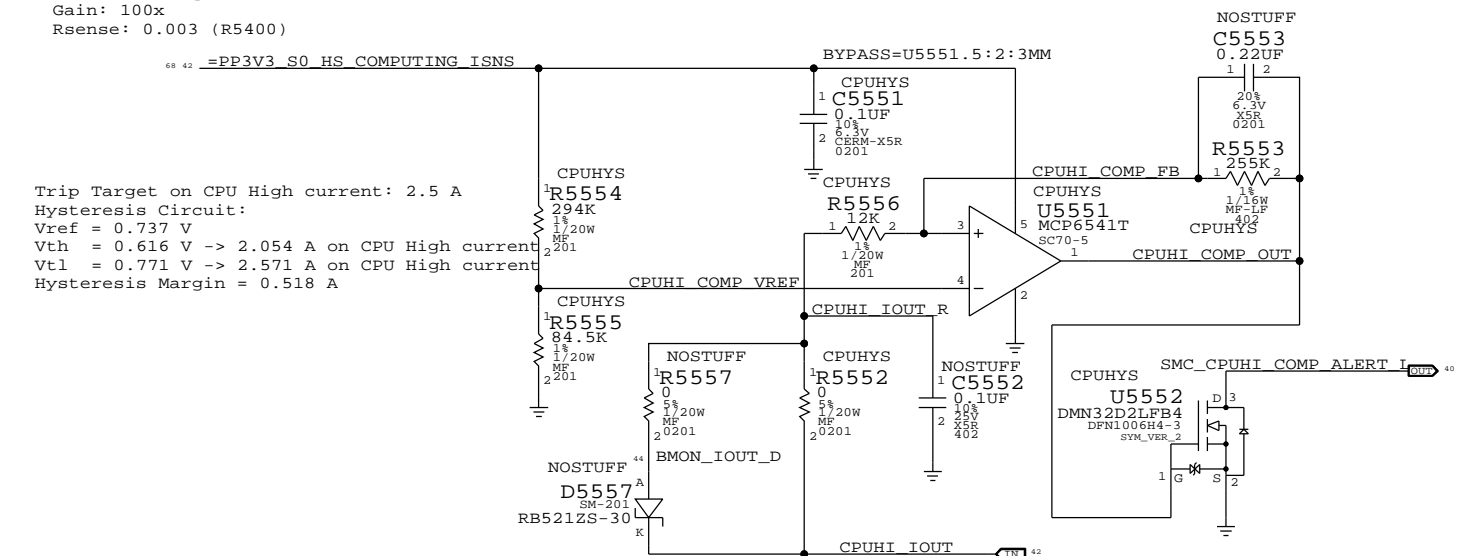
SSD Current Sense (ISDC)

Gain: 200x, EDP: 2.5 A (8.2 W)
Rsense: 0.005 (R5580)
Vsense: 12.5 mV, Range: 3.3 A
SMC ADC: 13



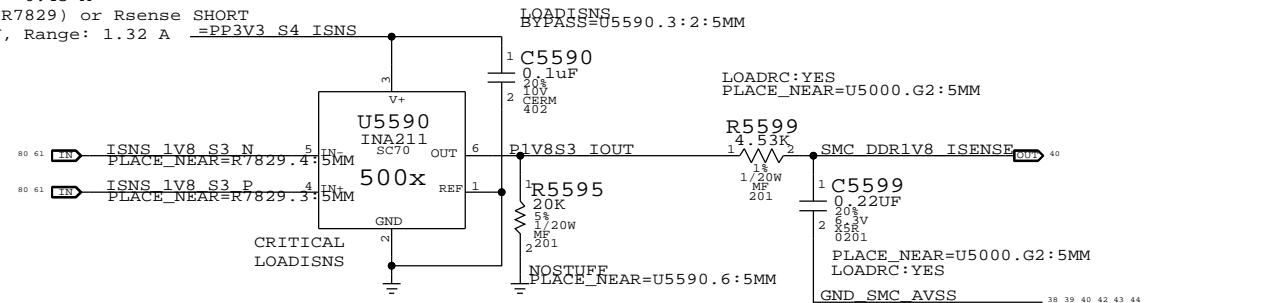
CPU High Side Current (IC0R) Threshold Alert

Gain: 100x
Rsense: 0.003 (R5400)



DDR 1.8V Current Sense (IM2C)

Gain: 500x, EDP: 0.45 A
Rsense: 0.005 (R7829) or Rsense SHORT
Vsense: 2.25 mV, Range: 1.32 A
SMC ADC: 12



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5569,C5519,C5599		LOADRC:NO
117S0008	3	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5529,C5539,C5549		LOADRC:NO
117S0008	1	RES,MTL,FLIM,100K,1/16W,0201,SMD,LF	C5579		DDRRC:NO

SYNC MASTER=JACK J52

SYNC DATE=12/06/2013

Power Sensors: Load Side

Apple Inc.

051-1573

8.0.0

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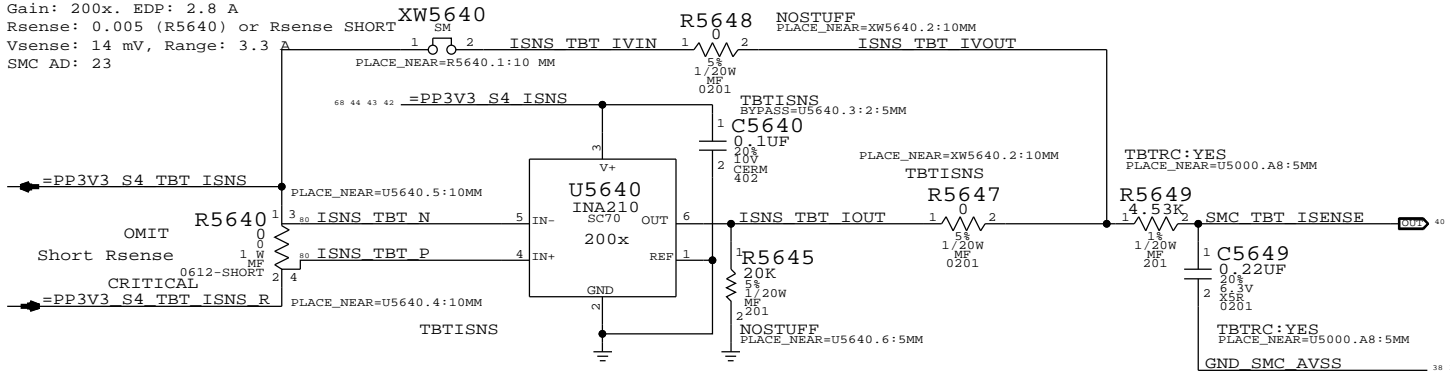
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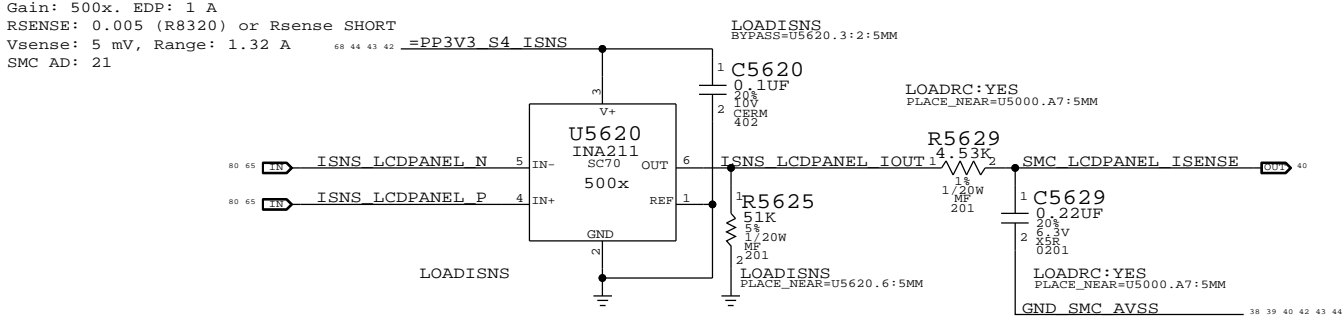
Thunderbolt TBT Current/Voltage Sense (IHSC/VHSC)



C

C

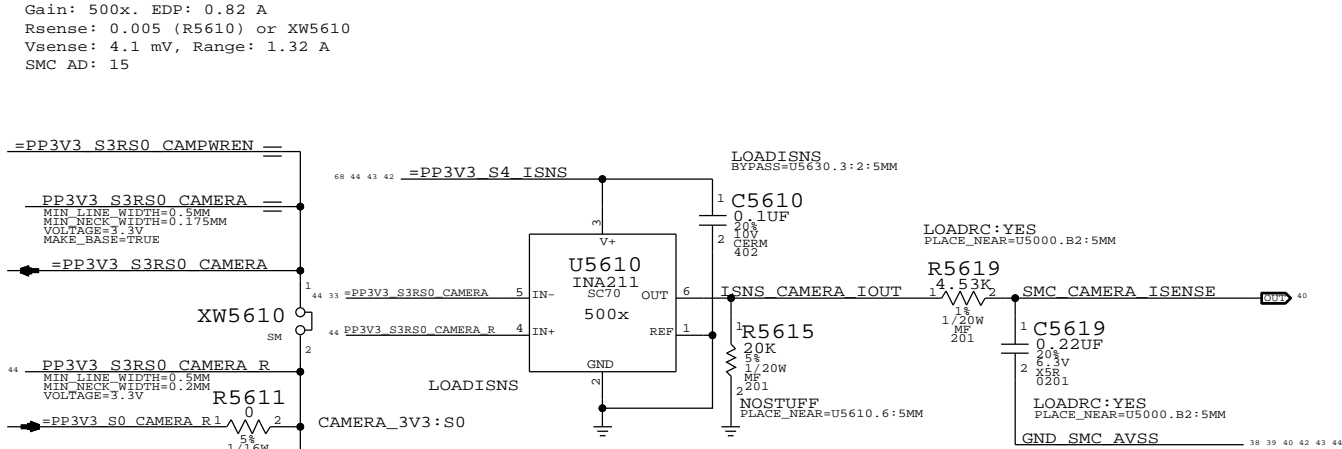
LCD Panel Current Sense (ILDC)



B

B

Camera (S2 Controller) Current Sense (ICMC)

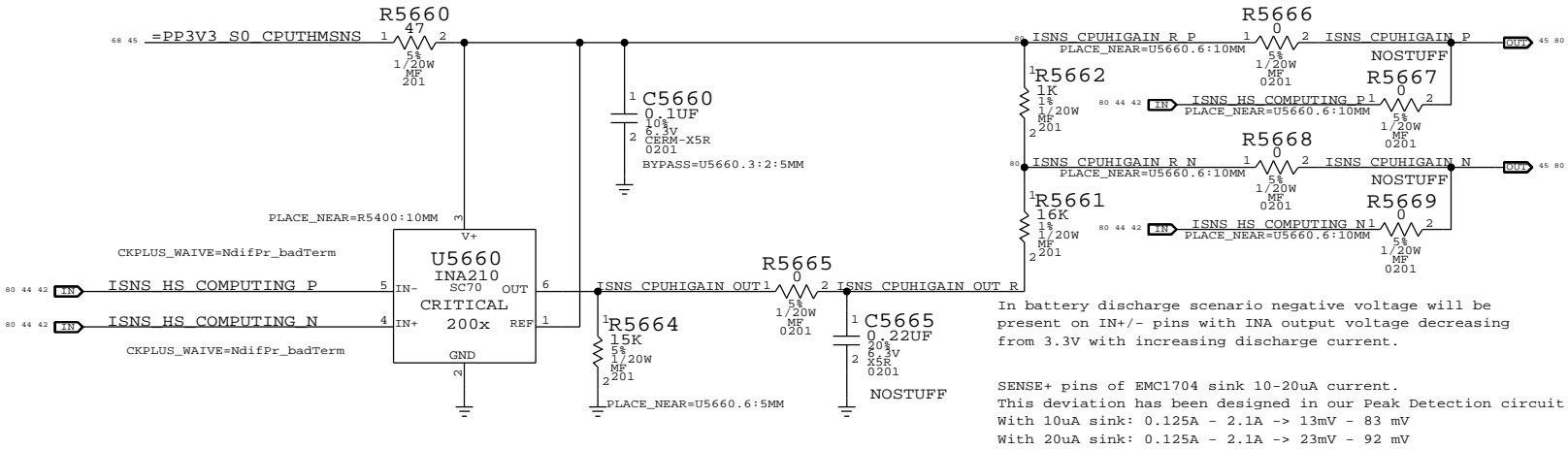


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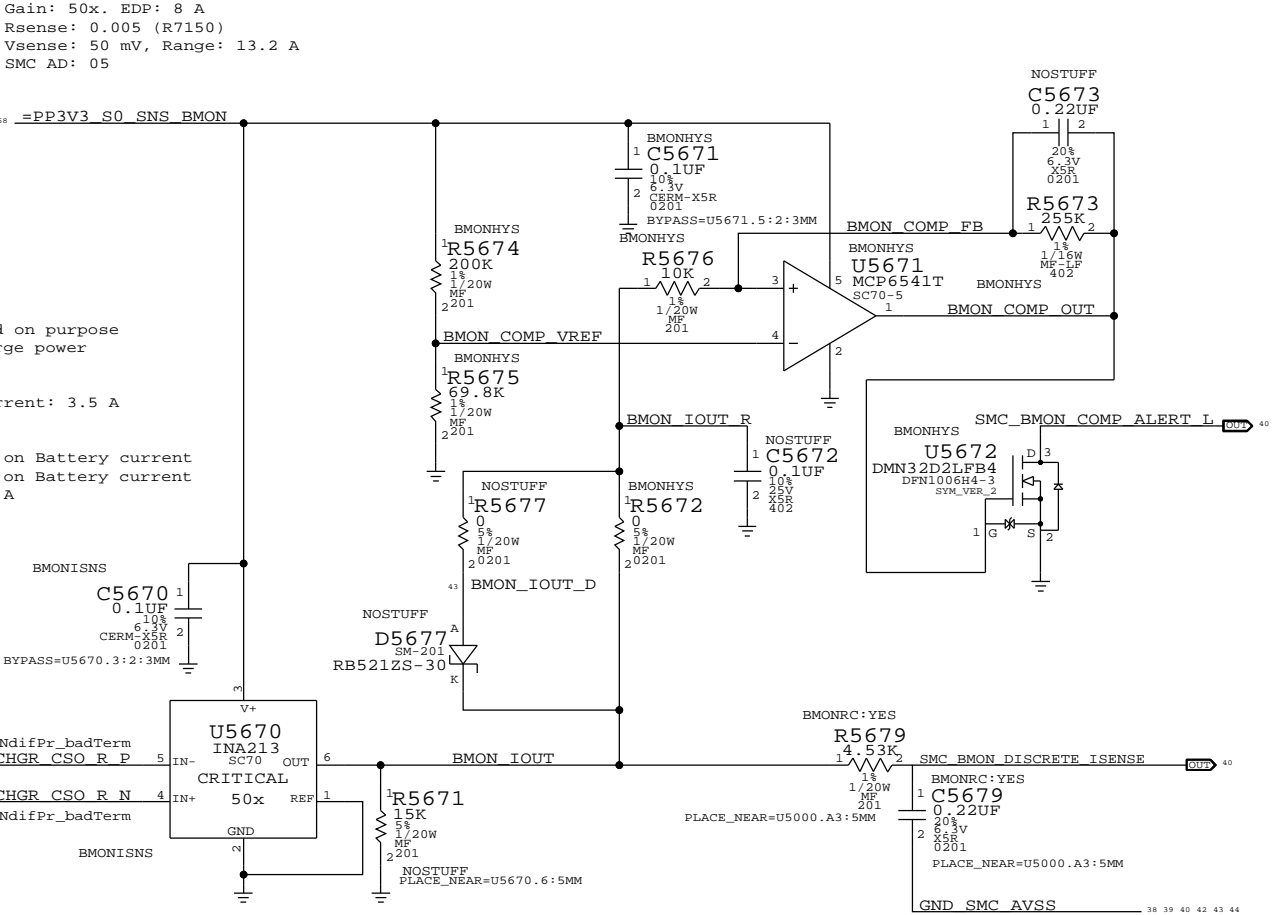
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5619,C5629		LOADRC:NO
117S0008	1	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5679		BMONRC:NO
117S0008	1	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5649		TBTRC:NO

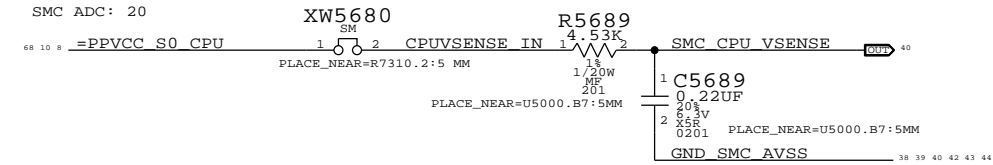
CPU High Side (IC0R) Peak Detection Support



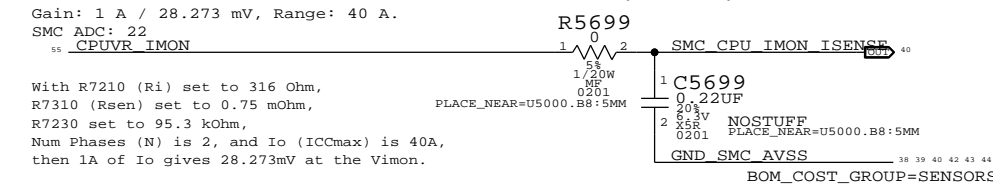
Battery BMON Discrete Current Sense (IP0R) & Threshold Alert




CPU Core Voltage Sense (VC0C)

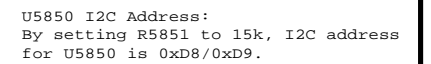


CPU Core IMON Current Sense (IC2C)



SYNC MASTER=JACK J52		SYNC DATE=10/26/2013	
PAGE TITLE			
Power Sensors: Extended		DRAWING NUMBER	
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		dvt1	
		PAGE	
		56 OF 120	
		SHEET	
		44 OF 82	

```
I2C Write: 0xD8, I2C Read: 0xD9
```

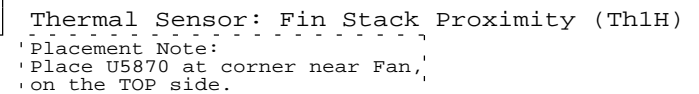


```

Thermal Diode: MLB Proximity (TMLB)
Placement Note:
Place U5850 on the TOP side, on the left portion
of the board, 1" to the right of USB connector.


```

I2C Write: 0x98, I2C Read: 0x99



NCX₁ C5800 0.0022UF 10% 50V CERM-X7R 0603 NCX₂

NCX₁ C5801 0.0022UF 10% 50V CERM-X7R 0603 NCX₂

SYMC MASTER-YHARTANTO J44		SYMC DATE=01/07/2015	
PAGE TITLE			
Thermal Sensors			
 Apple Inc.		DRAWING NUMBER	051-1573
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		SHEET	45 OF 82

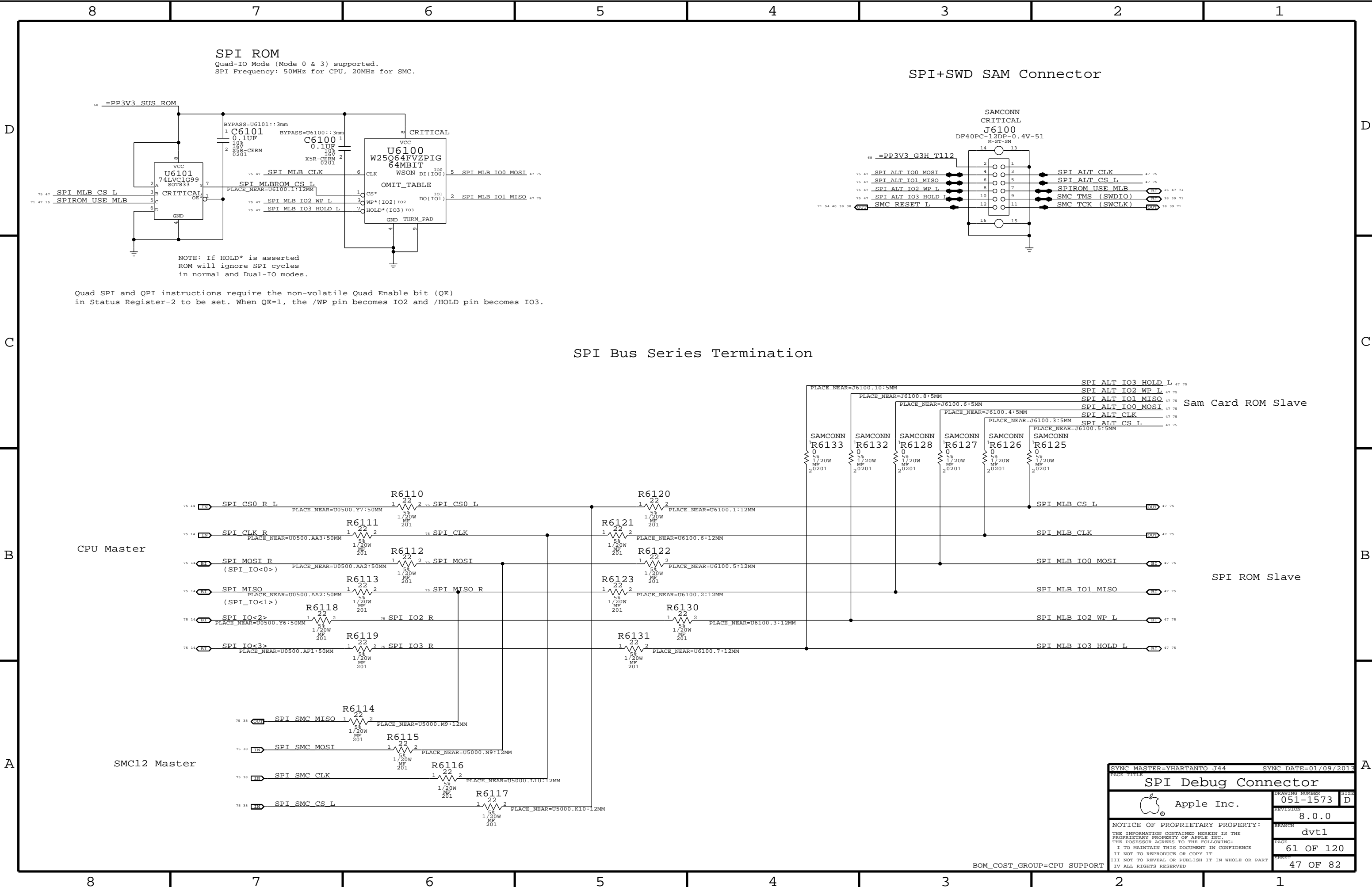
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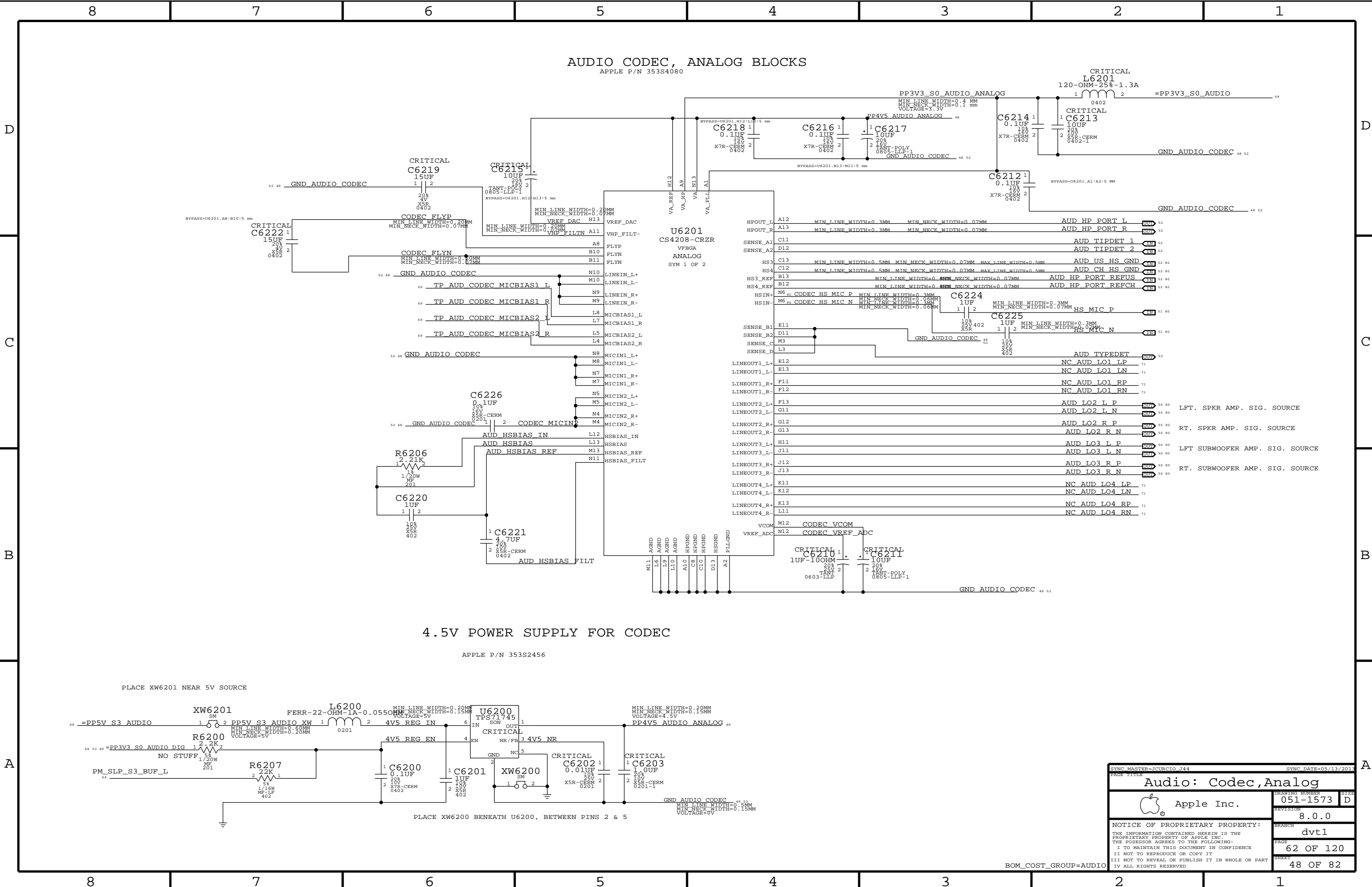
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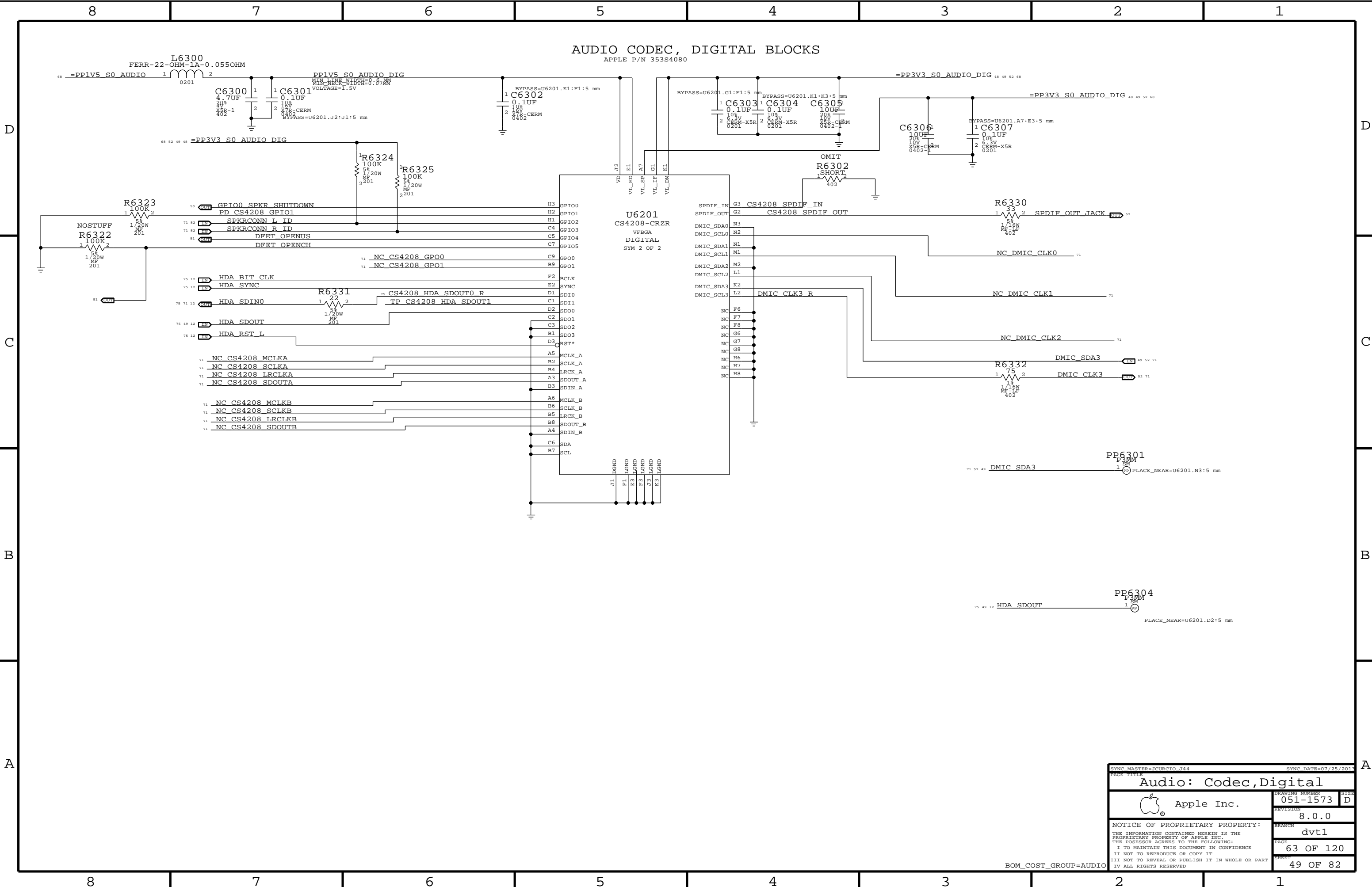
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BOM_COST_GROUP=FAN





SYNC MASTER=ICURCIO J44		SYNC DATE=05/13/2013	
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Audio: Codec, Analog			
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PAGE TITLE			
Audio: Codec,Digital		DRAWING NUMBER	
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4

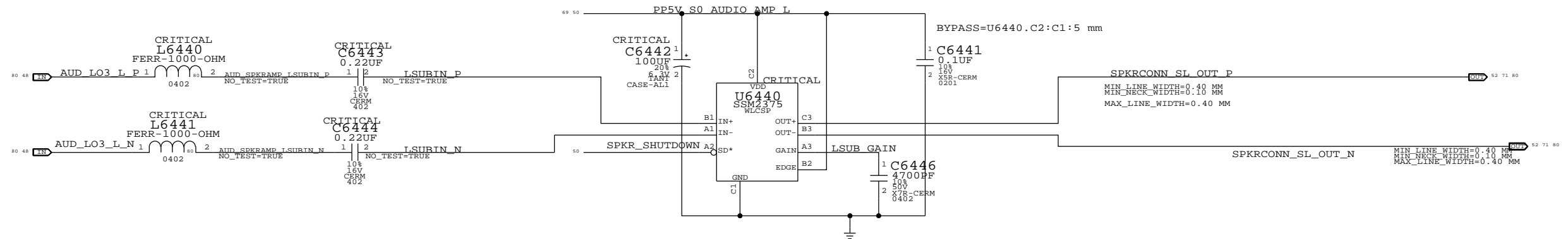
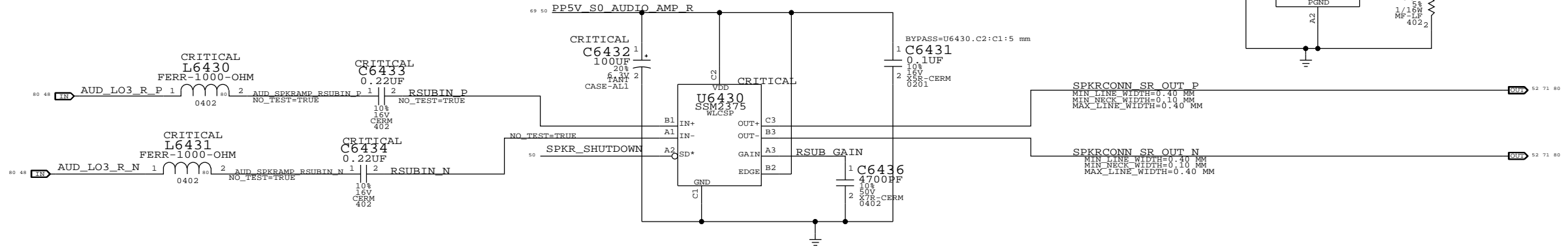
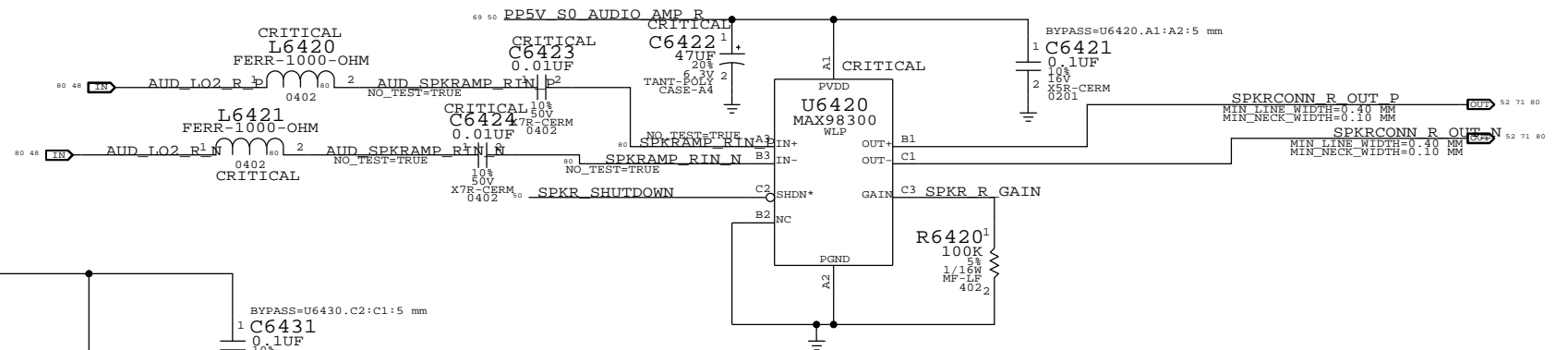
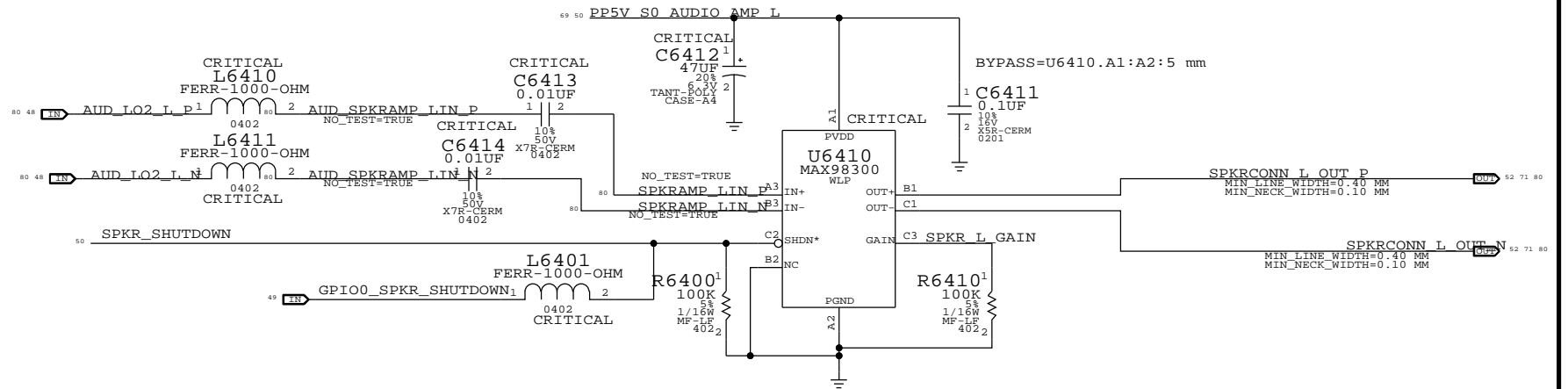
3

2

1

4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)

APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ

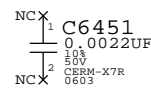
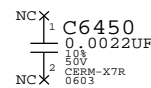
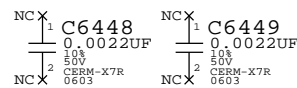
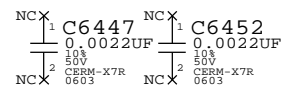


Placement Note: Place C6447 and C6452 near U6420


Placement Note: Place C6448 and C6449 near U6430

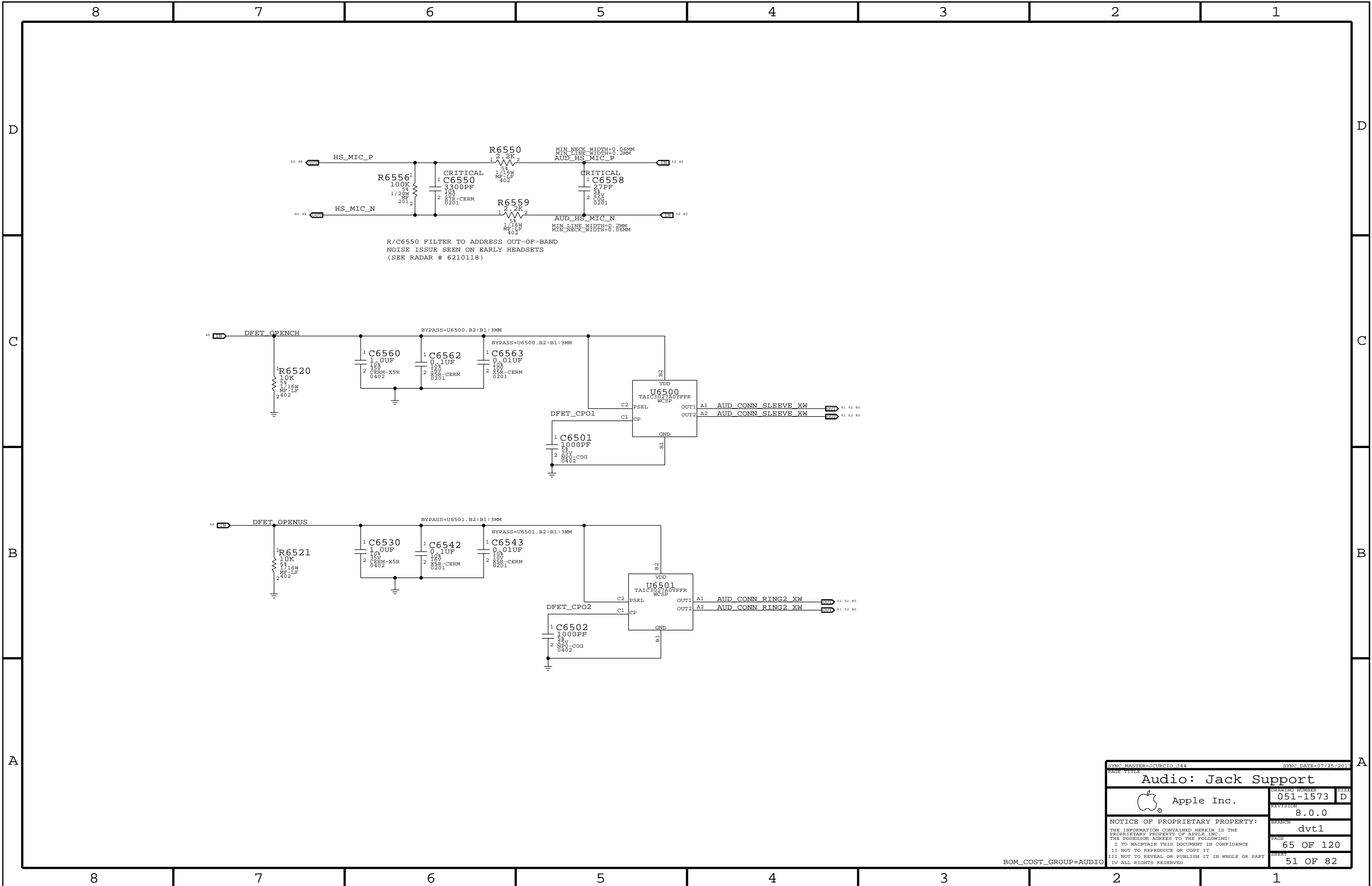
Placement Note: Place C6450 near U6410


Placement Note: Place C6451 near U6440



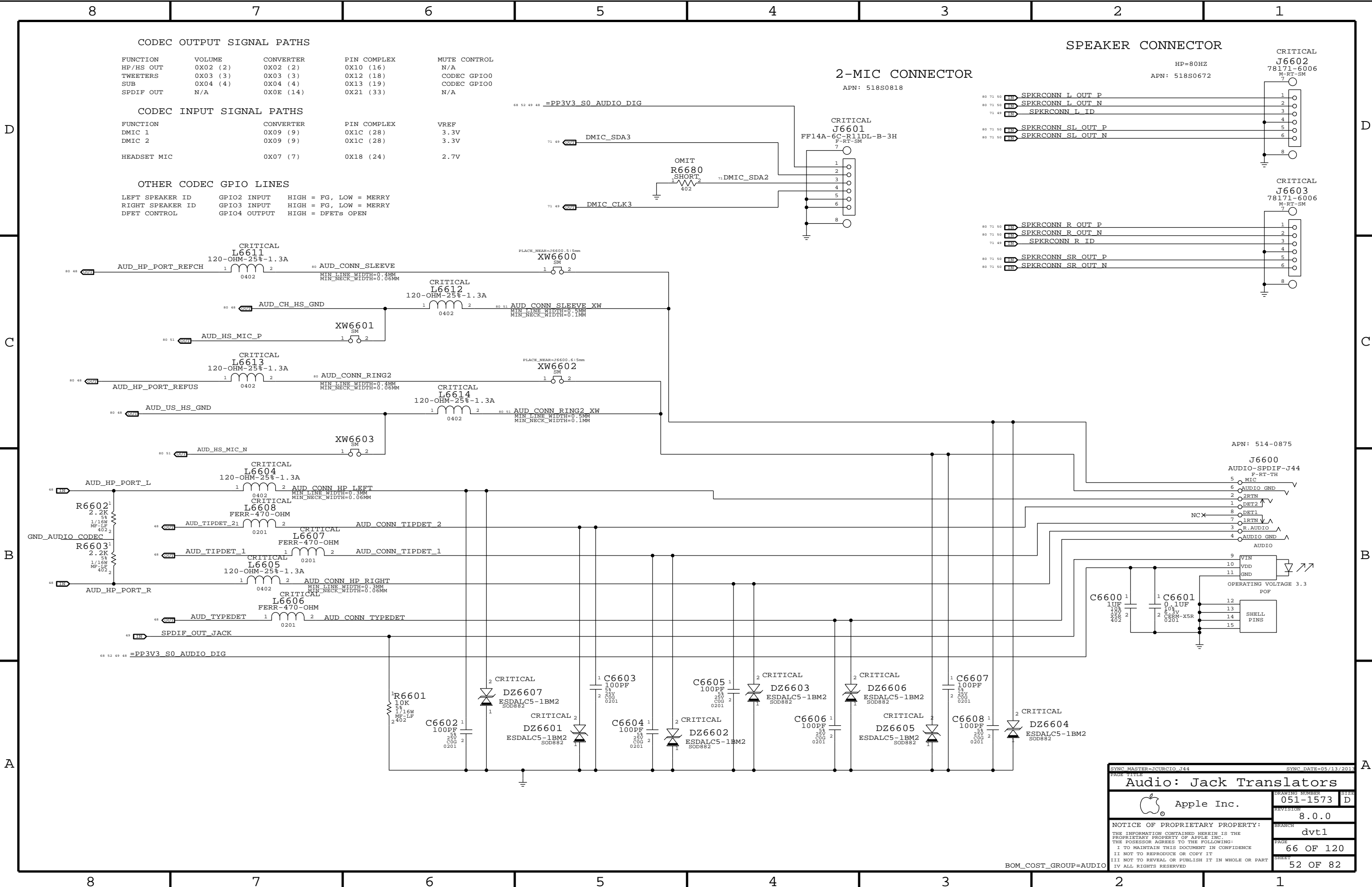
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SYNC MASTER=DIRK J44		SYNC DATE=01/09/2013	
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 Apple Inc.		SIZE	D
		REVISION	8.0.0
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Audio: Jack Support			
	Apple Inc.	DRAWING NUMBER	051-1573
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		PAGE	65 OF 120
		SHEET	51 OF 82

BOM_COST_GROUP=AUDIO



CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2 INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3 INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4 OUTPUT	HIGH = DFETs OPEN

2-MIC CONNECTOR

APN: 518S0818

SPEAKER CONNECTOR

HP=80HZ
APN: 518S0672

CRITICAL

J6602
78171-6006
M-RT-SM

CRITICAL

J6603
78171-6006
M-RT-SM

APN: 514-0875

J6600

AUDIO-SPDIF-J44

F-RT-TH

5 MIC

6 AUDIO GND

2 2RTN

1 DET2

8 DET1

7 1RTN

3 R.AUDIO

4 AUDIO GND

AUDIO

9 VIN

10 VDD

11 GND

OPERATING VOLTAGE 3.3

POF

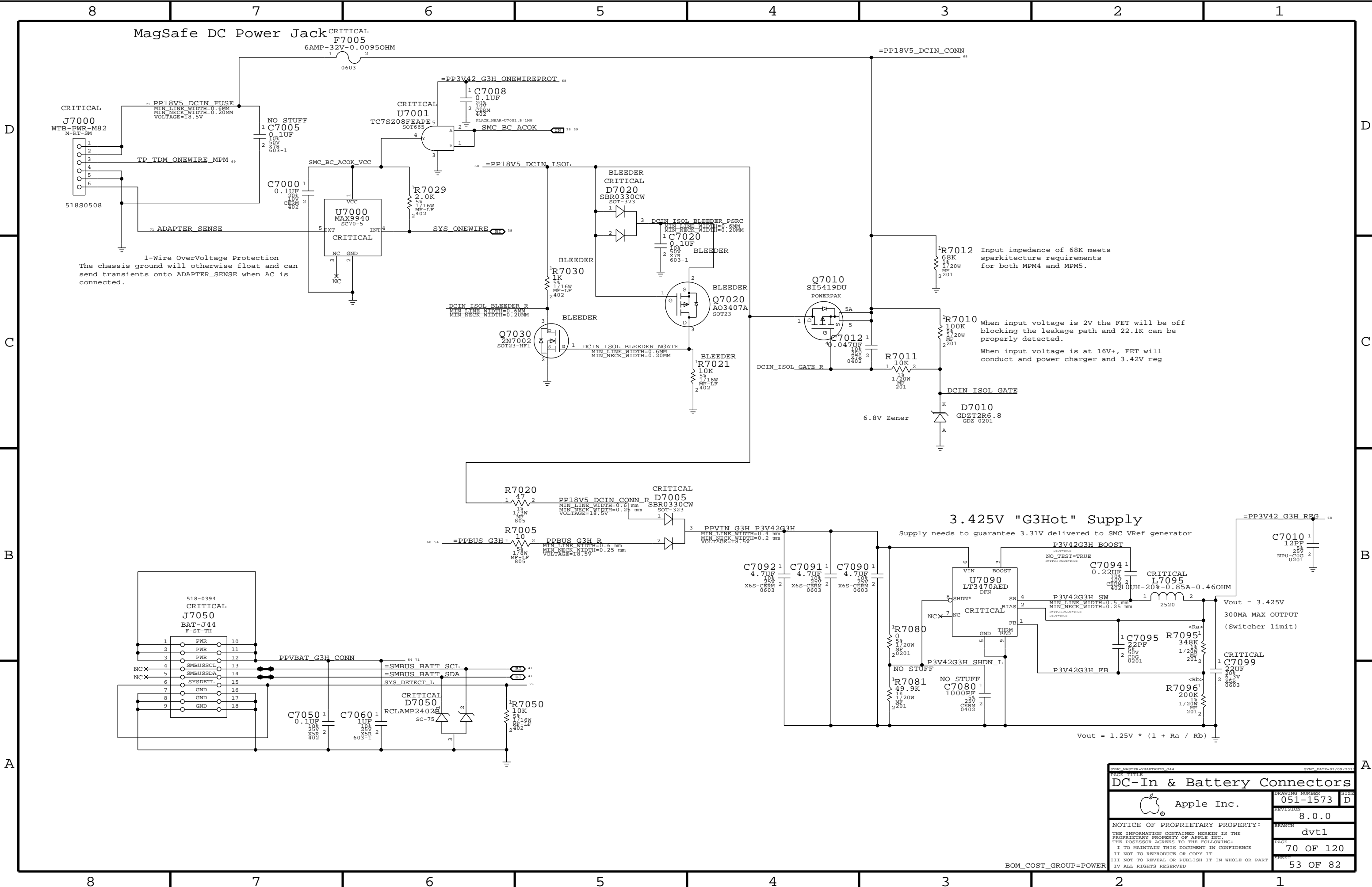
12 SHELL


14 PINS

15

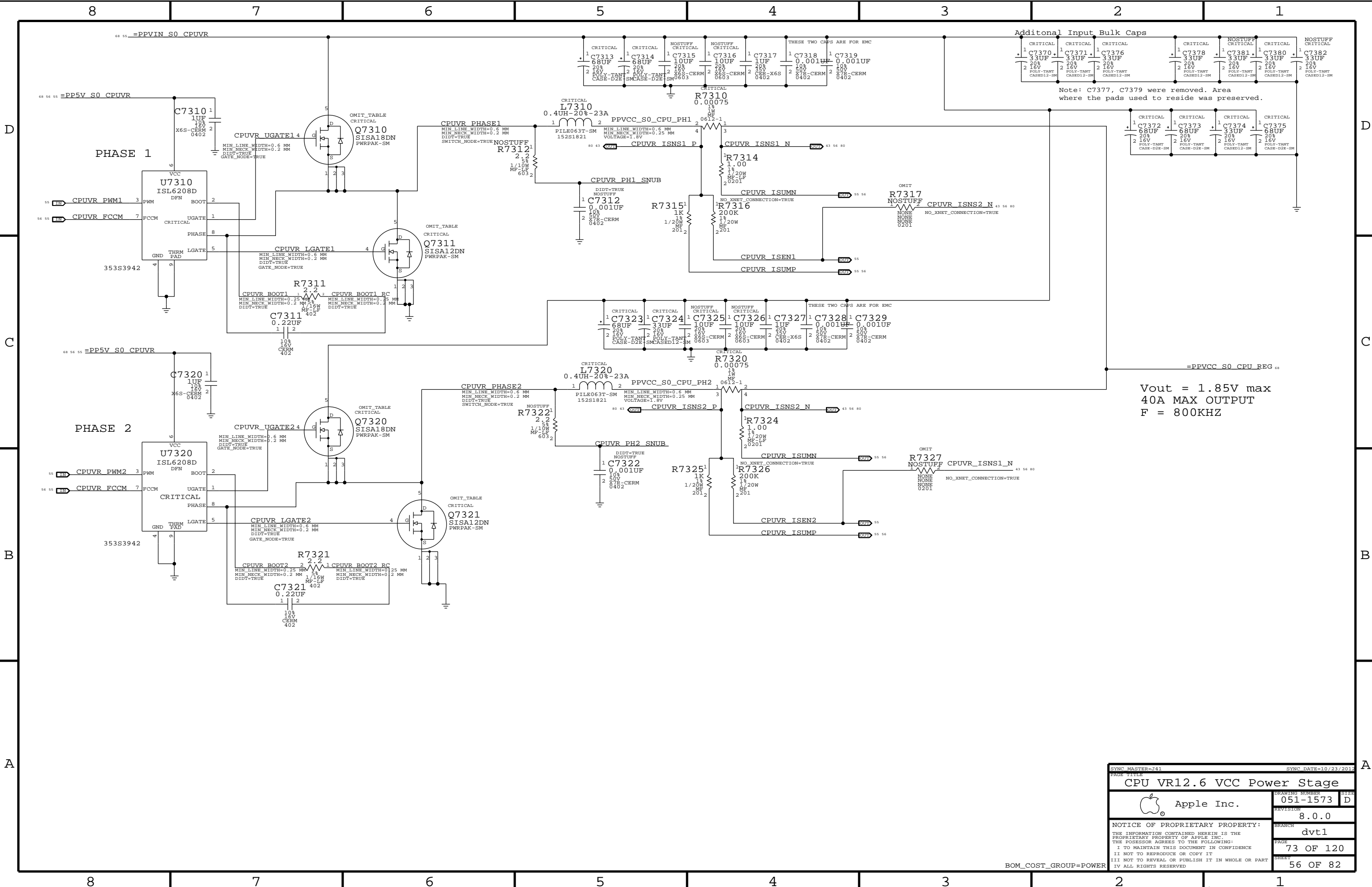
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Apple Inc.		DRAWING NUMBER	051-1573
		REVISION	8.0.0
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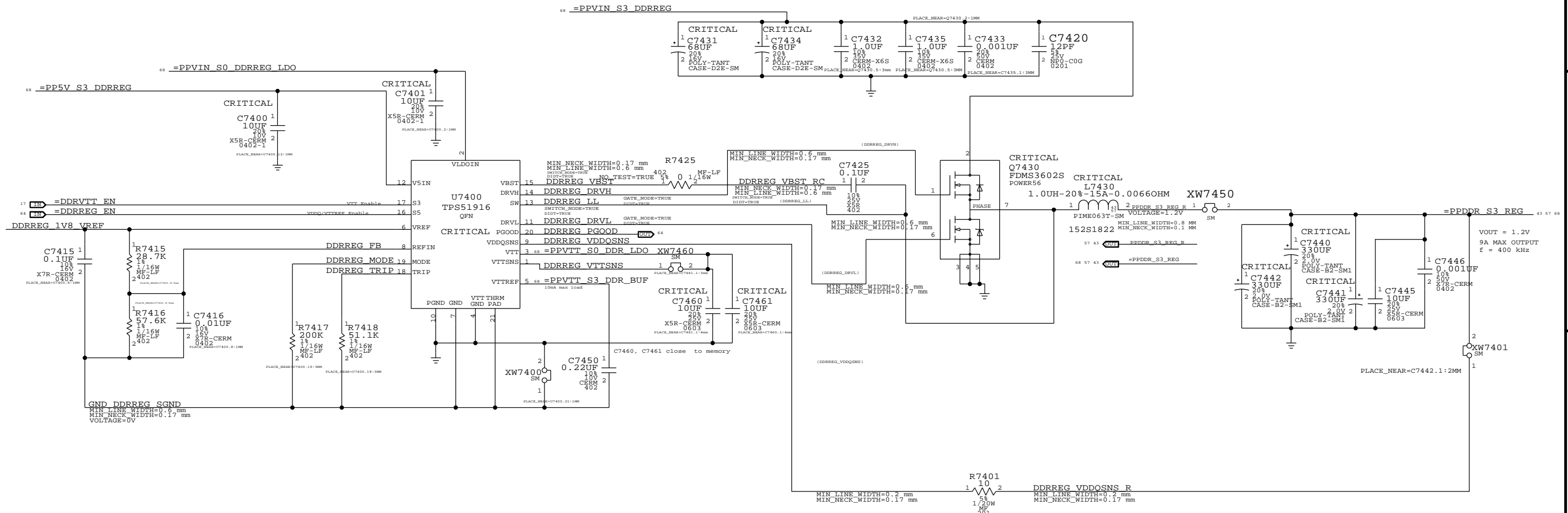
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		SHEET	53 OF 82






SYNC MASTER=J41		SYNC DATE=10/23/2012	
PAGE TITLE			
CPU VR12.6 VCC Power Stage			
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1.2V S3 Regulator



SYNC MASTER=J41 MLB		SYNC DATE=05/21/2013	
PAGE TITLE			
LPDDR3 Supply			
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		SIZE	D
		REVISION	8.0.0
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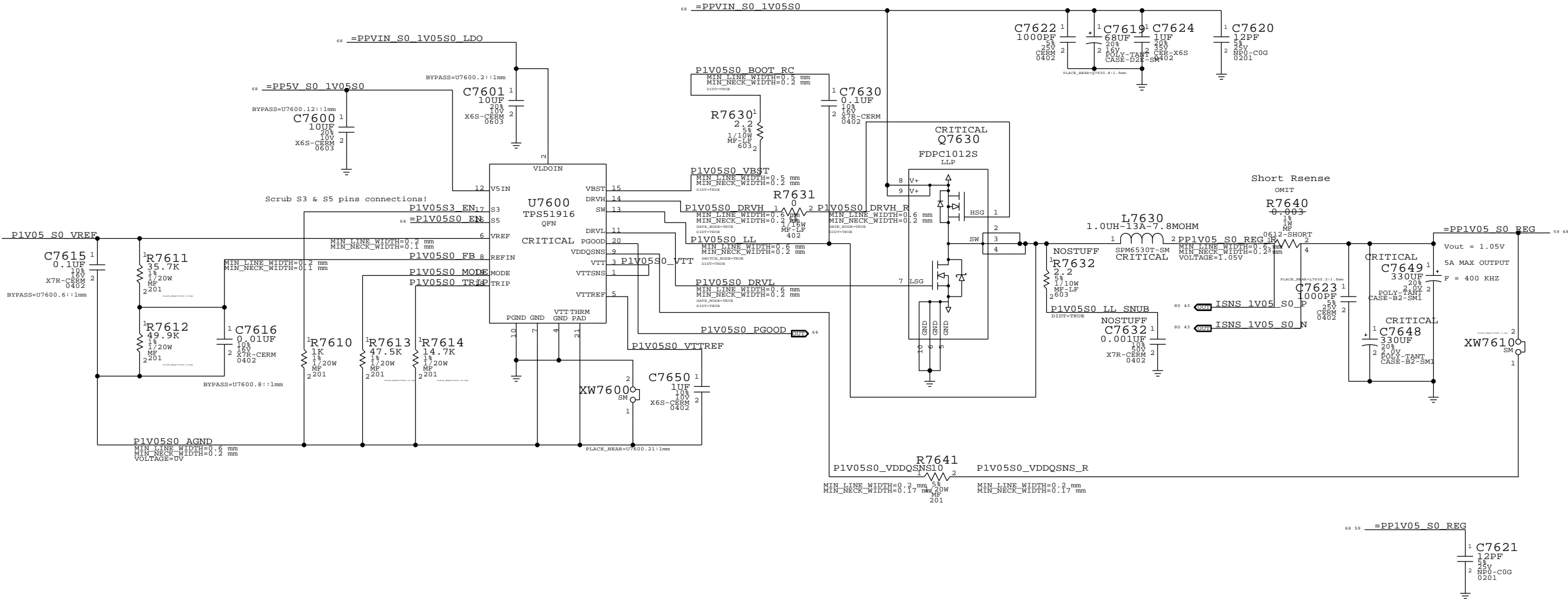
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1.05V S0 Regulator



SYNC MASTER=AHARTMAN J52		SYNC DATE=10/29/2013	
PAGE TITLE			
1.05V Power Supply			
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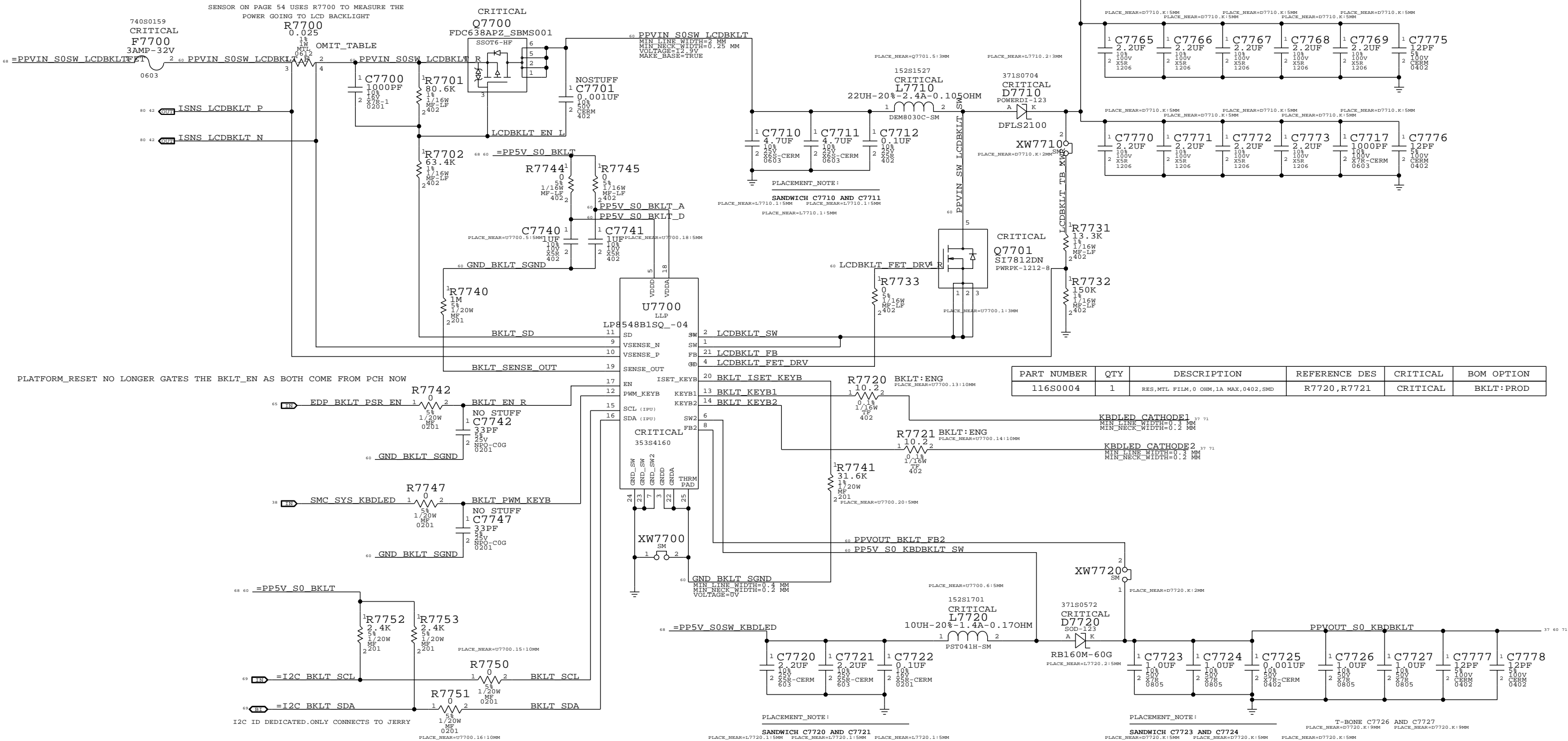
BOM_COST_GROUP=POWER

Page Notes

Power aliases required by this page:
 - =PPVIN_S0SW_LCDBKLT_FET (9-12.6V LCD BACKLIGHT INPUT)
 - =PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)
 - =PP5V_S0SW_KBDLED (5V KEYBOARD BACKLIGHT INPUT)

BOM options provided by this page:
 BKLT'ENG - Stuffs 10.2 ohm series R for engineering builds
 BKLT'PROD - Stuffs 0 ohm series R for production

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0386	RES,MTL	FILM,1W,25MOHM,1%,4TERM,0612,BLK	7700	CRITICAL	



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7720,R7721	CRITICAL	BKLT:PROD

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7720,R7721	CRITICAL	BKLT:PROD

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7720,R7721	CRITICAL	BKLT:PROD

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7720,R7721	CRITICAL	BKLT:PROD

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7720,R7721	CRITICAL	BKLT:PROD

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7720,R7721	CRITICAL	BKLT:PROD

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7720,R7721	CRITICAL	BKLT:PROD

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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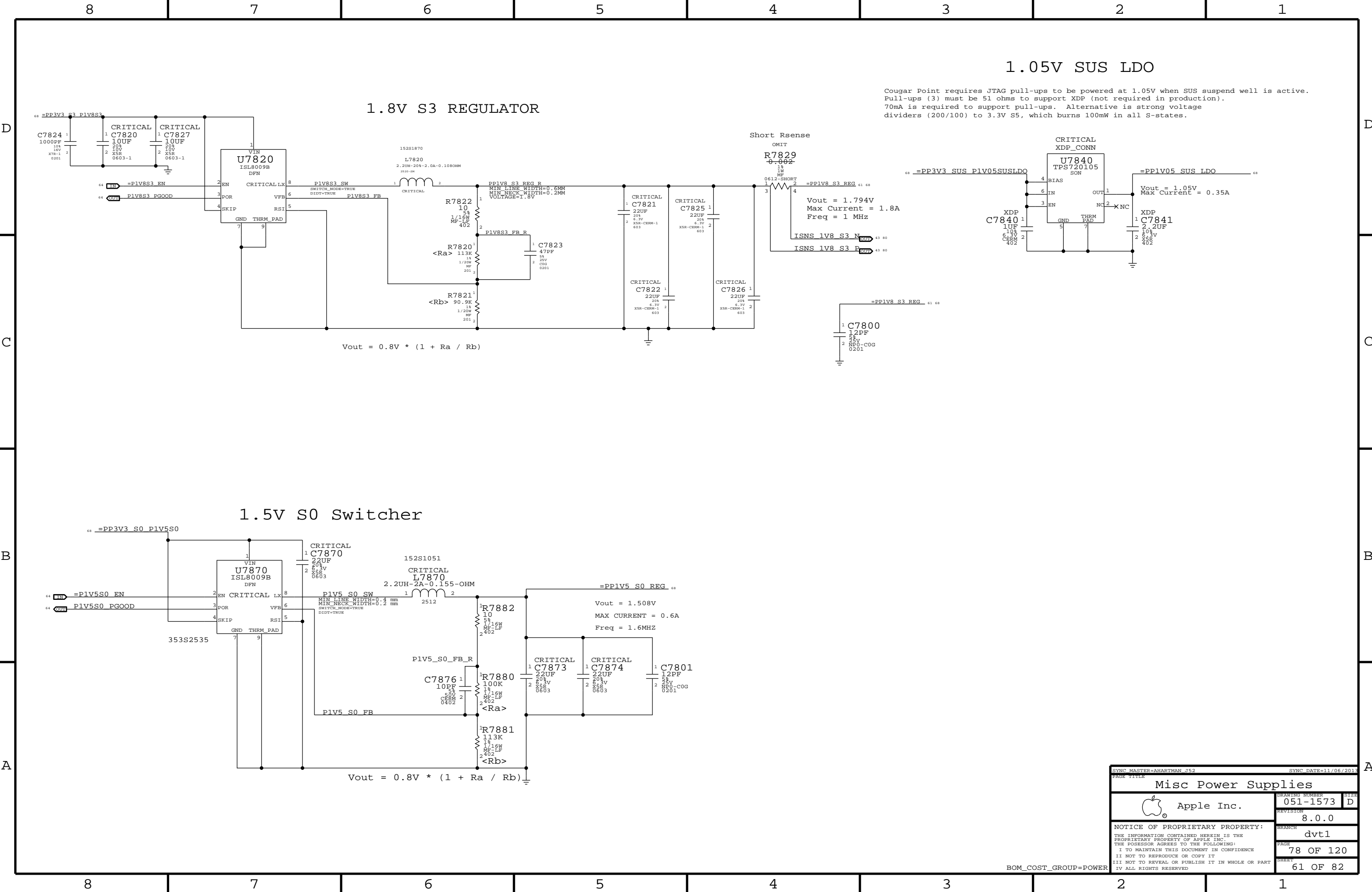
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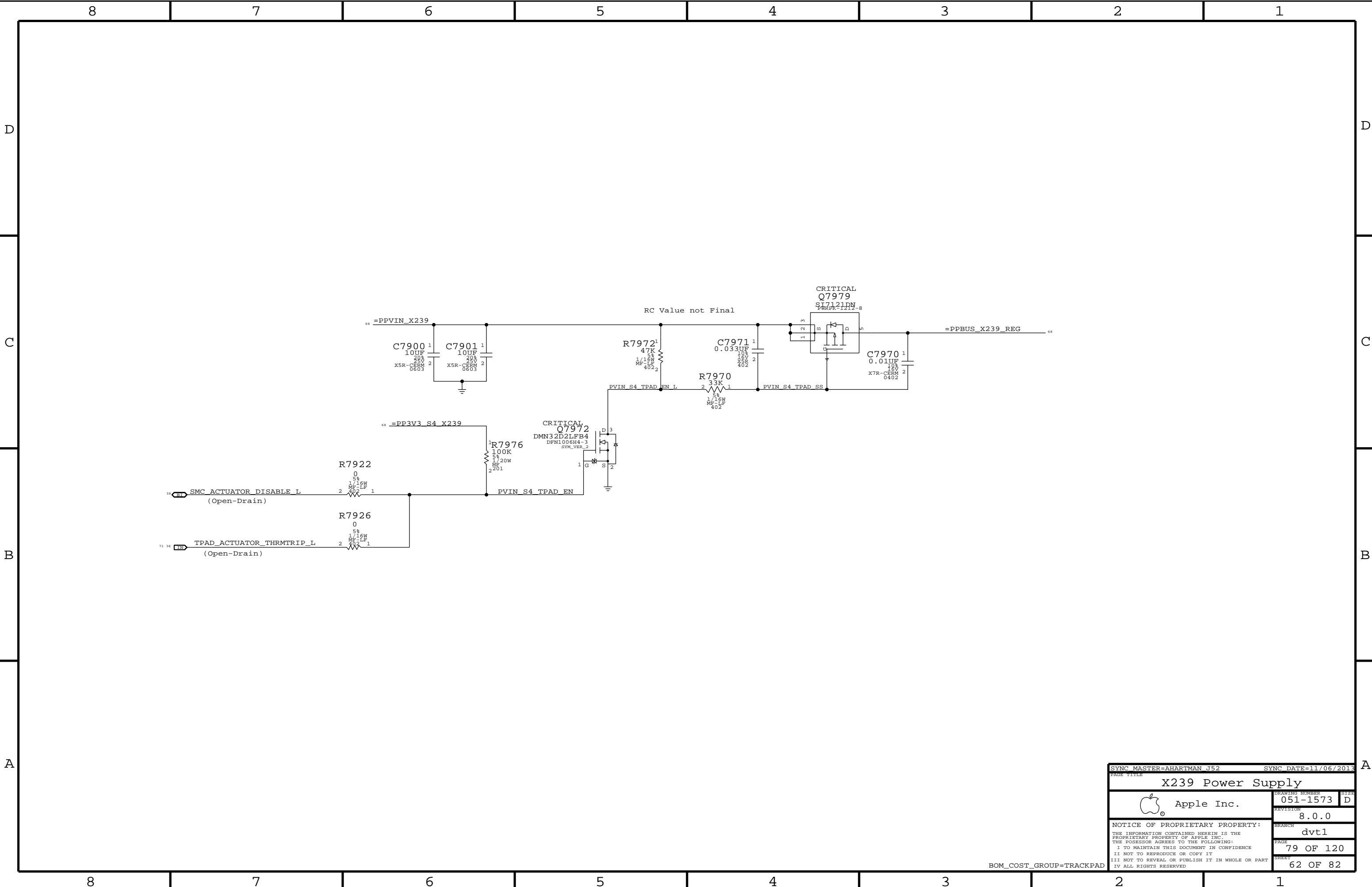
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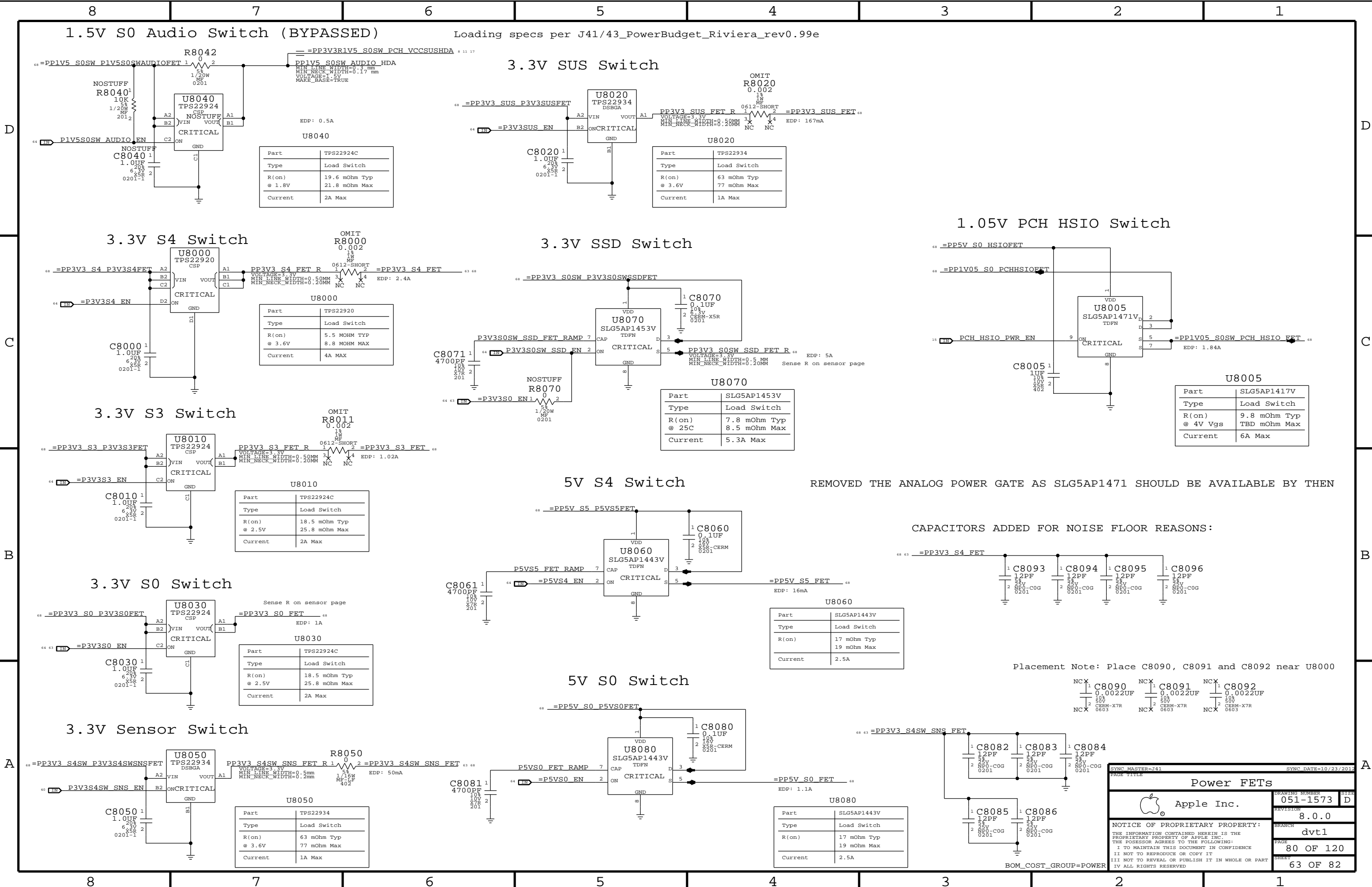


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X239 Power Supply			
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BOM_COST_GROUP=TRACKPAD



SYNC MASTER=J41

SYNC DATE=10/23/2012

Power FETs

Apple Inc.

051-1573

8.0.0

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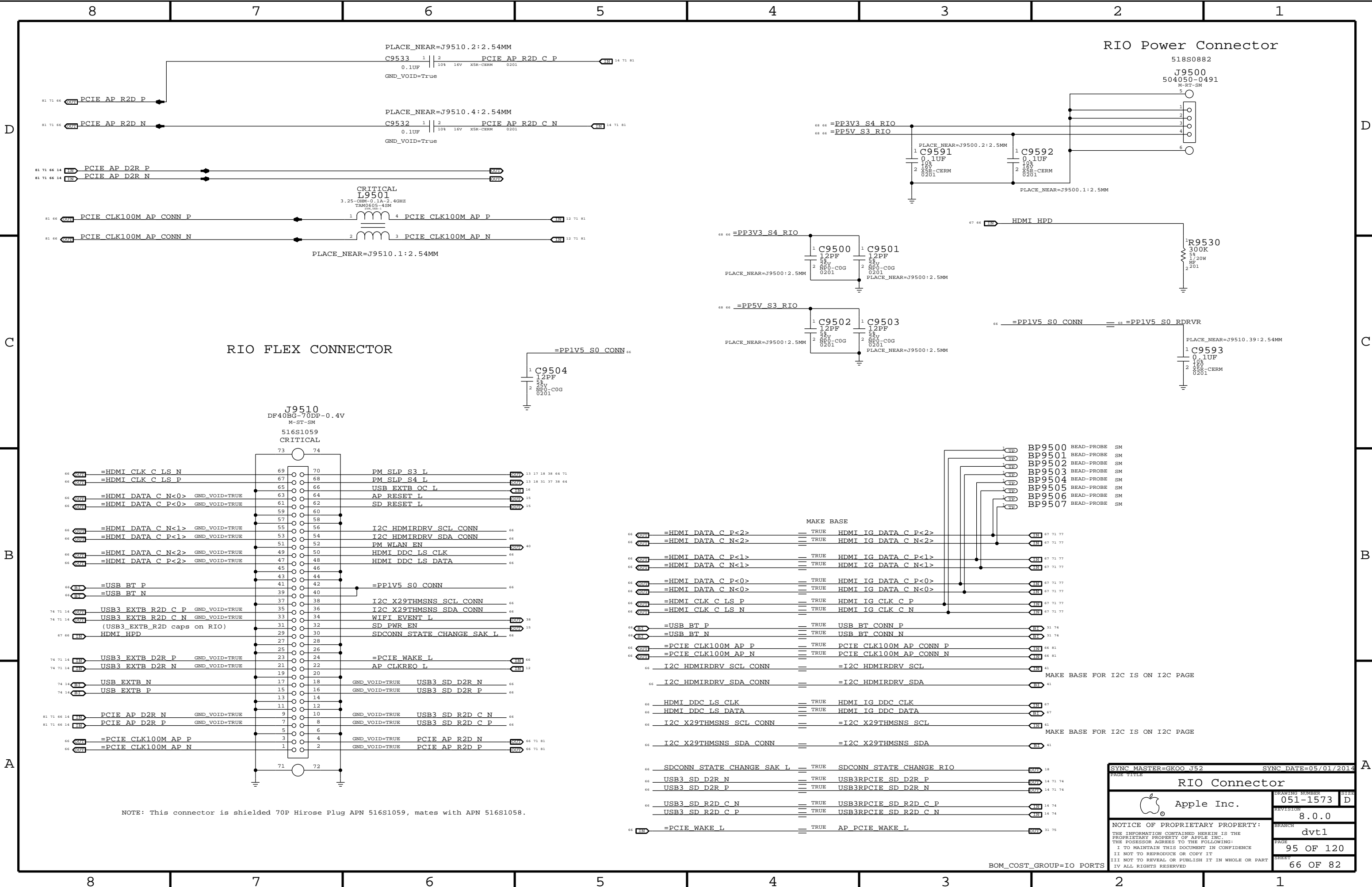
C




PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0007	1	RES,MF,1/20W,10K OHM,5,0201,SMD	R8342	CRITICAL	PANEL:OLD
117S0201	1	RES,MF,1A MAX,0.0 OHM,5%,0201,BLACK	R8342	CRITICAL	PANEL:NEW

8	7	6	5	4	3	2	1
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NOTE: This connector is shielded 70P Hirose Plug APN 516S1059, mates with APN 516S1058.

SYNC MASTER=GK00 J52		SYNC DATE=05/01/2014	
PAGE TITLE			
RIO Connector			
 Apple Inc.		DRAWING NUMBER	051-1573
		SIZE	D
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DISPLAY MUX: DP OR HDMI

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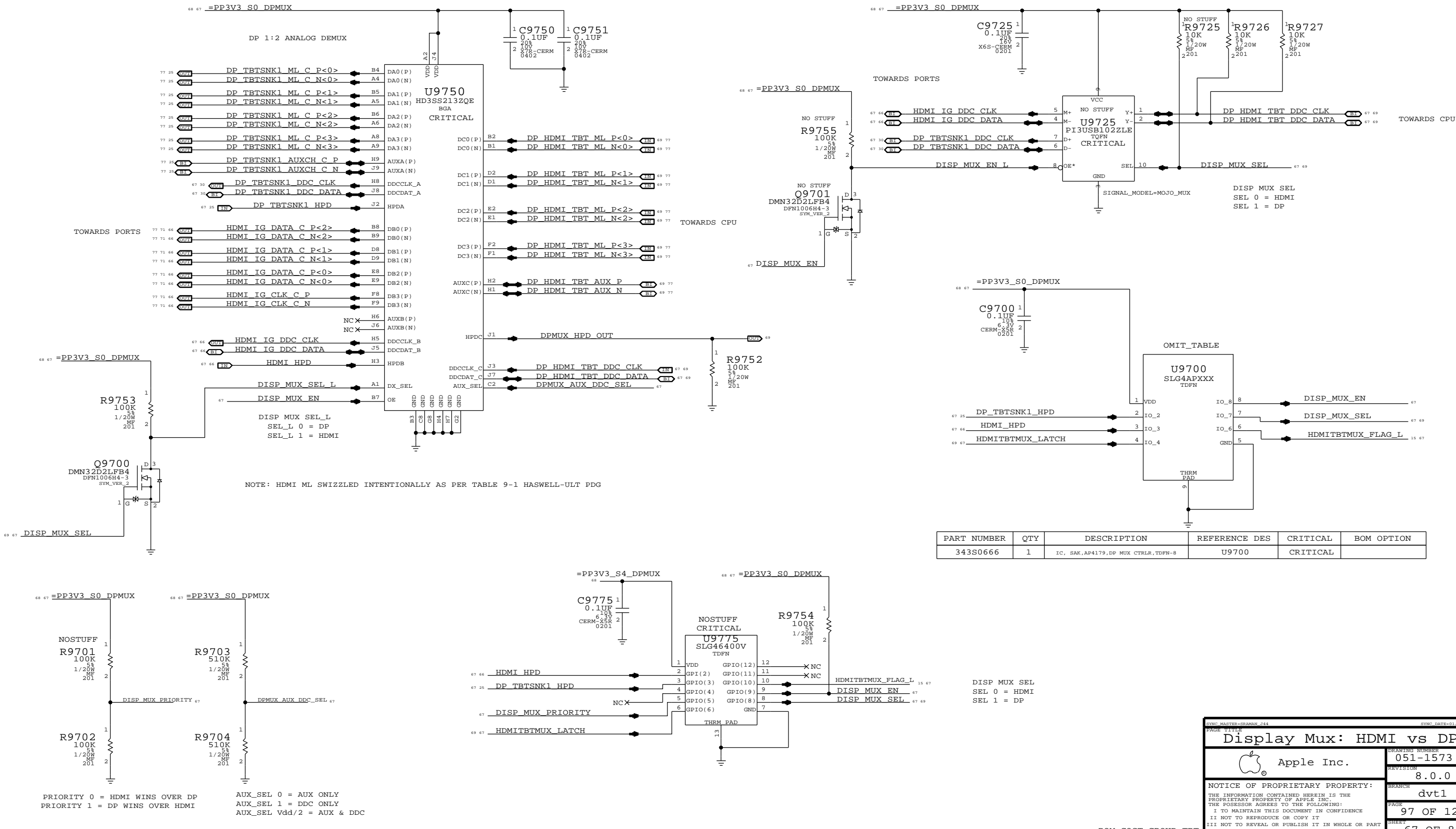
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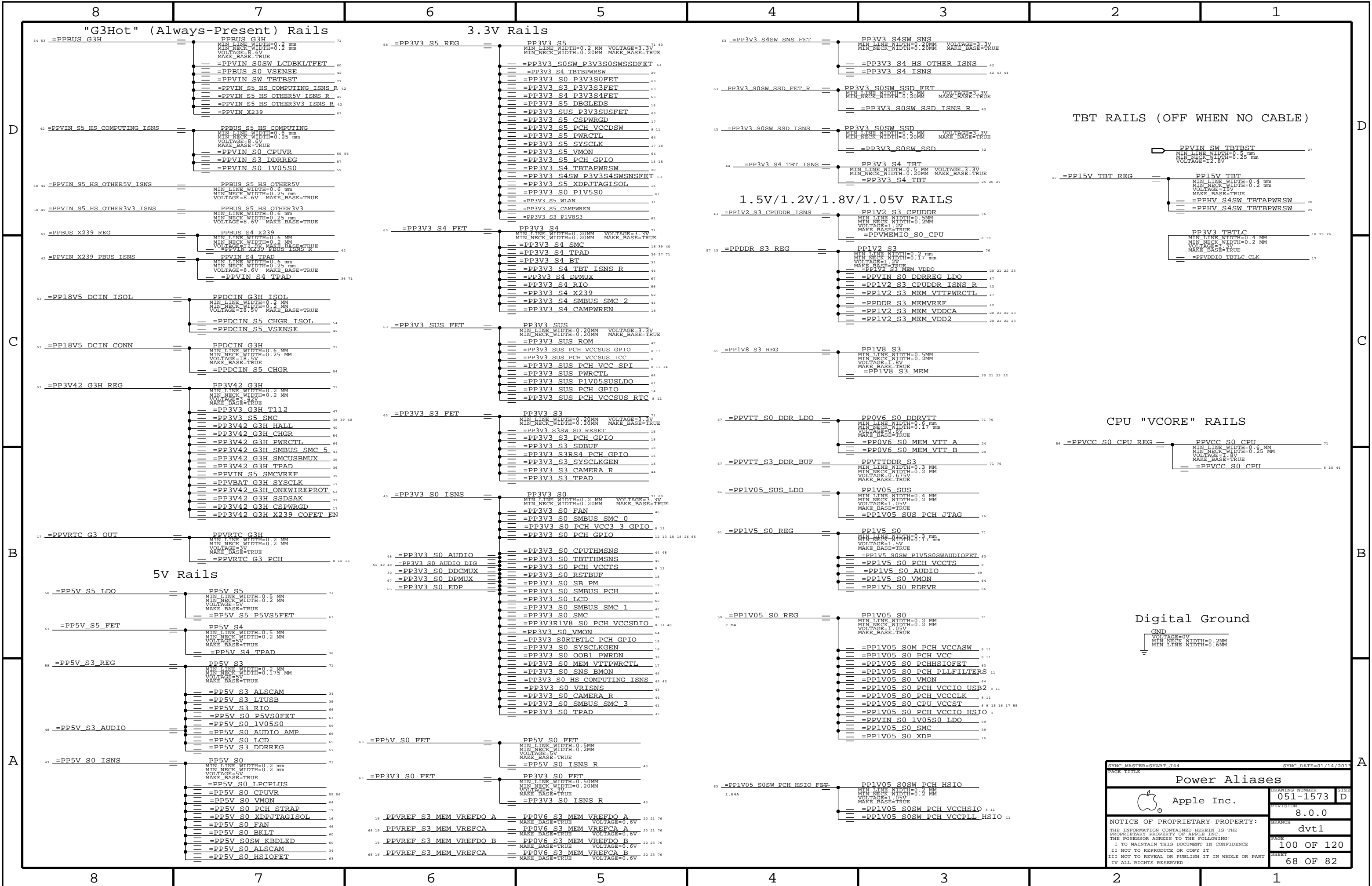
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0666	1	IC, SAK,AP4179,DP MUX CTRLR,TDFN-8	U9700	CRITICAL	

Display Mux: HDMI vs DP		DRAWING NUMBER	051-1573	SIZE	D
Apple Inc.		REVISION	8.0.0	BRANCH	dvt1
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HDMI VS TBT

```
MAKE_BASE
5 =DP TBTSNK1 ML C P<0> == TRUE DP HDMI TBT ML P<0> 67 77
5 =DP TBTSNK1 ML C N<0> == TRUE DP HDMI TBT ML N<0> 67 77
5 =DP TBTSNK1 ML C P<1> == TRUE DP HDMI TBT ML P<1> 67 77
5 =DP TBTSNK1 ML C N<1> == TRUE DP HDMI TBT ML N<1> 67 77
5 =DP TBTSNK1 ML C P<2> == TRUE DP HDMI TBT ML P<2> 67 77
5 =DP TBTSNK1 ML C N<2> == TRUE DP HDMI TBT ML N<2> 67 77
5 =DP TBTSNK1 ML C P<3> == TRUE DP HDMI TBT ML P<3> 67 77
5 =DP TBTSNK1 ML C N<3> == TRUE DP HDMI TBT ML N<3> 67 77
13 =DP TBTSNK1 AUXCH C P == TRUE DP HDMI TBT AUX P 67 77
13 =DP TBTSNK1 AUXCH C N == TRUE DP HDMI TBT AUX N 67 77
13 =DP TBTSNK1 DDC CLK == TRUE DP HDMI TBT DDC CLK 67
13 =DP TBTSNK1 DDC DATA == TRUE DP HDMI TBT DDC DATA 67
13 =DP TBTSNK1 HPD == TRUE DPMUX HPD OUT 67
```

```
25 HDMITBTMUX SEL TBT == =TBT GO2SX BIDIR 15
MAKE_BASE=TRUE
== DISP_MUX_SEL 67
13 DP AUXCH ISOL L == HDMITBTMUX LATCH 67
MAKE_BASE=TRUE
```

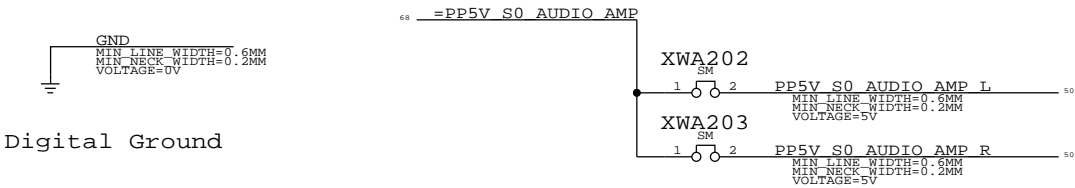
EPD PANEL

```
MAKE_BASE
60 =I2C BKLT_SCL == TRUE I2C BKLT_SCL 65 71
60 =I2C BKLT_SDA == TRUE I2C BKLT_SDA 65 71
```

UNUSED SIGNALS


```
MAKE_BASE
12 TP PCIE CLK100M FWP == TRUE NO_TEST=TRUE NC PCIE CLK100M FWP
12 TP PCIE CLK100M FWN == TRUE NO_TEST=TRUE NC PCIE CLK100M FWN
14 TP PCIE FW D2RP == TRUE NO_TEST=TRUE NC PCIE FW D2RP
14 TP PCIE FW D2RN == TRUE NO_TEST=TRUE NC PCIE FW D2RN
14 TP PCIE FW R2D CP == TRUE NO_TEST=TRUE NC PCIE FW R2D CP
14 TP PCIE FW R2D CN == TRUE NO_TEST=TRUE NC PCIE FW R2D CN
12 TP PCIE CLK100M ENETSDP == TRUE NO_TEST=TRUE NC PCIE CLK100M ENETSDP
12 TP PCIE CLK100M ENETSDN == TRUE NO_TEST=TRUE NC PCIE CLK100M ENETSDN
14 USB IR P == TRUE NO_TEST=TRUE NC USB IRP 74
14 USB IR N == TRUE NO_TEST=TRUE NC USB IRN 74
14 TP USB CAMERAP == TRUE NO_TEST=TRUE NC USB CAMERAP 74
14 TP USB CAMERAN == TRUE NO_TEST=TRUE NC USB CAMERAN 74
14 TP USB SDP == TRUE NO_TEST=TRUE NC USB SDP 74
14 TP USB SDN == TRUE NO_TEST=TRUE NC USB SDN 74
12 TP HDA SDIN1 == TRUE NO_TEST=TRUE NC HDA SDIN1
12 TP PCI PME L == TRUE NO_TEST=TRUE NC PCI PME L
14 TP CLINK CLK == TRUE NO_TEST=TRUE NC CLINK CLK
14 TP CLINK DATA == TRUE NO_TEST=TRUE NC CLINK DATA
14 TP CLINK RESET L == TRUE NO_TEST=TRUE NC CLINK RESET L
12 TP ITPXDP CLK100MN == TRUE NO_TEST=TRUE NC ITPXDP CLK100MN
12 TP ITPXDP CLK100MP == TRUE NO_TEST=TRUE NC ITPXDP CLK100MP
12 TP PCH I2S1 TXD == TRUE NO_TEST=TRUE NC PCH I2S1 TXD
12 TP PCH I2S1 SFRM == TRUE NO_TEST=TRUE NC PCH I2S1 SFRM
12 TP PCH I2S1 SCLK == TRUE NO_TEST=TRUE NC PCH I2S1 SCLK
13 TP PCH SLP WLAN L == TRUE NO_TEST=TRUE NC PCH SLP WLAN L
13 TP PCH SLP LAN L == TRUE NO_TEST=TRUE NC PCH SLP LAN L
14 TP SPI CS1 L == TRUE NO_TEST=TRUE NC SPI CS1 L
14 TP SPI CS2 L == TRUE NO_TEST=TRUE NC SPI CS2 L
14 TP USB 5N == TRUE NO_TEST=TRUE NC USB 5N 74
14 TP USB 5P == TRUE NO_TEST=TRUE NC USB 5P 74
```

```
48 TP AUD CODEC MICBIAS1 L == TRUE NO_TEST=TRUE NC AUD CODEC MICBIAS1 L
48 TP AUD CODEC MICBIAS1 R == TRUE NO_TEST=TRUE NC AUD CODEC MICBIAS1 R
48 TP AUD CODEC MICBIAS2 L == TRUE NO_TEST=TRUE NC AUD CODEC MICBIAS2 L
48 TP AUD CODEC MICBIAS2 R == TRUE NO_TEST=TRUE NC AUD CODEC MICBIAS2 R
64 TP SUS PGOOD MR L == TRUE NO_TEST=TRUE NC SUS PGOOD MR L
TP SMC TRST L == TRUE NO_TEST=TRUE NC SMC TRST L
TP SMC MD1 == TRUE NO_TEST=TRUE NC SMC MD1
53 TP TDM ONEWIRE MPM == TRUE NO_TEST=TRUE NC TDM ONEWIRE MPM
```



TBT UNUSED NETS

```
25 TP TBT MONDC0 == TRUE NC TBT MONDC0
25 TP TBT MONDC1 == MAKE_BASE=TRUE NC TBT MONDC1
25 TP TBT PCIE RESET0 L == MAKE_BASE=TRUE NC TBT PCIE RESET0 L
25 TP TBT XTAL25OUT == MAKE_BASE=TRUE NC TBT XTAL25OUT
25 TP DP TBTSRC ML CP<3> == TRUE NC DP TBTSRC ML CP<3>
25 TP DP TBTSRC ML CN<3> == MAKE_BASE=TRUE NC DP TBTSRC ML CN<3>
25 TP DP TBTSRC ML CP<2> == TRUE NC DP TBTSRC ML CP<2>
25 TP DP TBTSRC ML CN<2> == MAKE_BASE=TRUE NC DP TBTSRC ML CN<2>
25 TP DP TBTSRC ML CP<1> == TRUE NC DP TBTSRC ML CP<1>
25 TP DP TBTSRC ML CN<1> == MAKE_BASE=TRUE NC DP TBTSRC ML CN<1>
25 TP DP TBTSRC ML CP<0> == TRUE NC DP TBTSRC ML CP<0>
25 TP DP TBTSRC ML CN<0> == MAKE_BASE=TRUE NC DP TBTSRC ML CN<0>
25 TP DP TBTSRC AUXCH CP == TRUE NC DP TBTSRC AUXCH CP
25 TP DP TBTSRC AUXCH CN == MAKE_BASE=TRUE NC DP TBTSRC AUXCH CN
```

SYNC MASTER=SHART J44		SYNC DATE=11/19/2012	
PAGE TITLE			
Signal Aliases			
 Apple Inc.		DRAWING NUMBER	051-1573
		REVISION	8.0.0
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X304 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS							
BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA, P65BGA, BGA_MEM		MM	16.5
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.190 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.120 MM	0.120 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL2, ISL11	Y	0.120 MM	0.120 MM		0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.155 MM	0.155 MM		0.125 MM	0.125 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
73_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.110 MM	0.110 MM		0.120 MM	0.120 MM
73_OHM_DIFF	ISL2, ISL11	Y	0.110 MM	0.110 MM		0.120 MM	0.120 MM
73_OHM_DIFF	TOP,BOTTOM	Y	0.141 MM	0.141 MM		0.120 MM	0.120 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1T01_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?


Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3, ISL4, ISL9, ISL10	0.053 MM	?
1X_DIELECTRIC	ISL2, ISL5, ISL6, ISL7, ISL8, ISL11	0.101 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

SYNC MASTER=YHARTANTO J44			SYNC DATE=12/14/2012		
PAGE TITLE			PCB Rule Definitions		
 Apple Inc.			DRAWING NUMBER	051-1573	SIZE D
			REVISION	8.0.0	
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USB 2 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIA5	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?	USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIA5	*	=6X_DIELECTRIC	?	USB_RBIA5	TOP,BOTTOM	=10X_DIELECTRIC	?

USB 3 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?	USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?	USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?	USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	*	*	USB3_2OTHER
USB3_*	=SAME	*	USB3_2SAME
USB3_TX	*_RX	*	USB3_TXRX
USB3_RX	*_TX	*	USB3_TXRX

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5x_DIELECTRIC	?


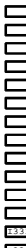







SATA Interface Constraints (Not Used)

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?	SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?	SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?	SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	*	*	SATA_2OTHER
SATA_*	=SAME	*	SATA_2SAME
SATA_TX	*_RX	*	SATA_TXRX
SATA_RX	*_TX	*	SATA_TXRX

USB Constraints

ELECTRICAL CONST SET		NET TYPE				
		PHYSICAL	SPACING			
	USB_BT	USB_85D	USB	USB_BT_P	14 31	
	USB_BT	USB_85D	USB	USB_BT_N	14 31	
	USB_BT	USB_85D	USB	USB_BT_CONN_P	31 66	
	USB_BT	USB_85D	USB	USB_BT_CONN_N	31 66	
	USB_EXT_A	USB_85D	USB	USB_EXT_A_P	14 35	
	USB_EXT_A	USB_85D	USB	USB_EXT_A_N	14 35	
		DEFAULT	DEFAULT	SMC_DEBUGPRT_RX_L	35 38	
		DEFAULT	DEFAULT	SMC_DEBUGPRT_TX_L	35 38	
	USB_EXT_A	USB_85D	USB	USB2_EXT_A_MUXED_P	35	
	USB_EXT_A	USB_85D	USB	USB2_EXT_A_MUXED_N	35	
	USB_EXT_A	USB_85D	USB	USB2_EXT_A_MUXED_F_P	35	
	USB_EXT_A	USB_85D	USB	USB2_EXT_A_MUXED_F_N	35	
	USB_EXT_A	USB_85D	USB	USB_LT1_P	71	
	USB_EXT_A	USB_85D	USB	USB_LT1_N	71	
	USB_EXT_B	USB_85D	USB	USB_EXT_B_P	14 66	
	USB_EXT_B	USB_85D	USB	USB_EXT_B_N	14 66	
	USB_TPAD	USB_85D	USB	USB_TPAD_P	14 36 71	
	USB_TPAD	USB_85D	USB	USB_TPAD_N	14 36 71	
		USB3_EXT_A_D2R	USB_85D	USB3_RX	USB3_EXT_A_D2R_P	14 35 71
USB3_EXT_A_D2R		USB_85D	USB3_RX	USB3_EXT_A_D2R_N	14 35 71	
USB3_EXT_A_R2D		USB_85D	USB3_TX	USB3_EXT_A_R2D_P	35	
USB3_EXT_A_R2D		USB_85D	USB3_TX	USB3_EXT_A_R2D_N	35 71	
USB3_EXT_A_R2D		USB_85D	USB3_TX	USB3_EXT_A_R2D_C_P	14 35 71	
USB3_EXT_A_R2D		USB_85D	USB3_TX	USB3_EXT_A_R2D_C_N	14 35 71	
USB3_EXT_B_D2R		USB_85D	USB3_RX	USB3_EXT_B_D2R_P	14 66 71	
USB3_EXT_B_D2R		USB_85D	USB3_RX	USB3_EXT_B_D2R_N	14 66 71	
USB3_EXT_B_R2D		USB_85D	USB3_TX	USB3_EXT_B_R2D_C_P	14 66 71	
USB3_EXT_B_R2D		USB_85D	USB3_TX	USB3_EXT_B_R2D_C_N	14 66 71	
	USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE_SD_D2R_P	14 66 71	
	USB3_SD_D2R	USB3_85D	USB3_RX	USB3RPCIE_SD_D2R_N	14 66 71	
	USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE_SD_R2D_C_P	14 66	
	USB3_SD_R2D	USB3_85D	USB3_TX	USB3RPCIE_SD_R2D_C_N	14 66	
	USB_NC	USB_85D	USB	NC_USB_IRP	69	
	USB_NC	USB_85D	USB	NC_USB_IRN	69	
	USB_NC	USB_85D	USB	NC_USB_5P	69	
	USB_NC	USB_85D	USB	NC_USB_5N	69	
	USB_NC	USB_85D	USB	NC_USB_SDP	69	
	USB_NC	USB_85D	USB	NC_USB_SDN	69	
	USB_NC	USB_85D	USB	NC_USB_CAMERAP	69	
	USB_NC	USB_85D	USB	NC_USB_CAMERAN	69	
	PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	14	
		SATA_85D	SATA_RX	DUMMY_SATA_D2R_P		
		SATA_85D	SATA_RX	DUMMY_SATA_D2R_N		
		SATA_85D	SATA_TX	DUMMY_SATA_R2D_P		
		SATA_85D	SATA_TX	DUMMY_SATA_R2D_N		
	SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	17	
	SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	17	
	SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	17	
	SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	17 34	
	SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKP	33 34	
	SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R	34	
	SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP	34	
	SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN	34	
	SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	17 25	
	SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	25	

Notes:
This is here to keep the SATA rules.

SYNC MASTER=YHARTANTO J44

SYNC DATE=01/07/2013

USB Constraints

Apple Inc.

051-1573

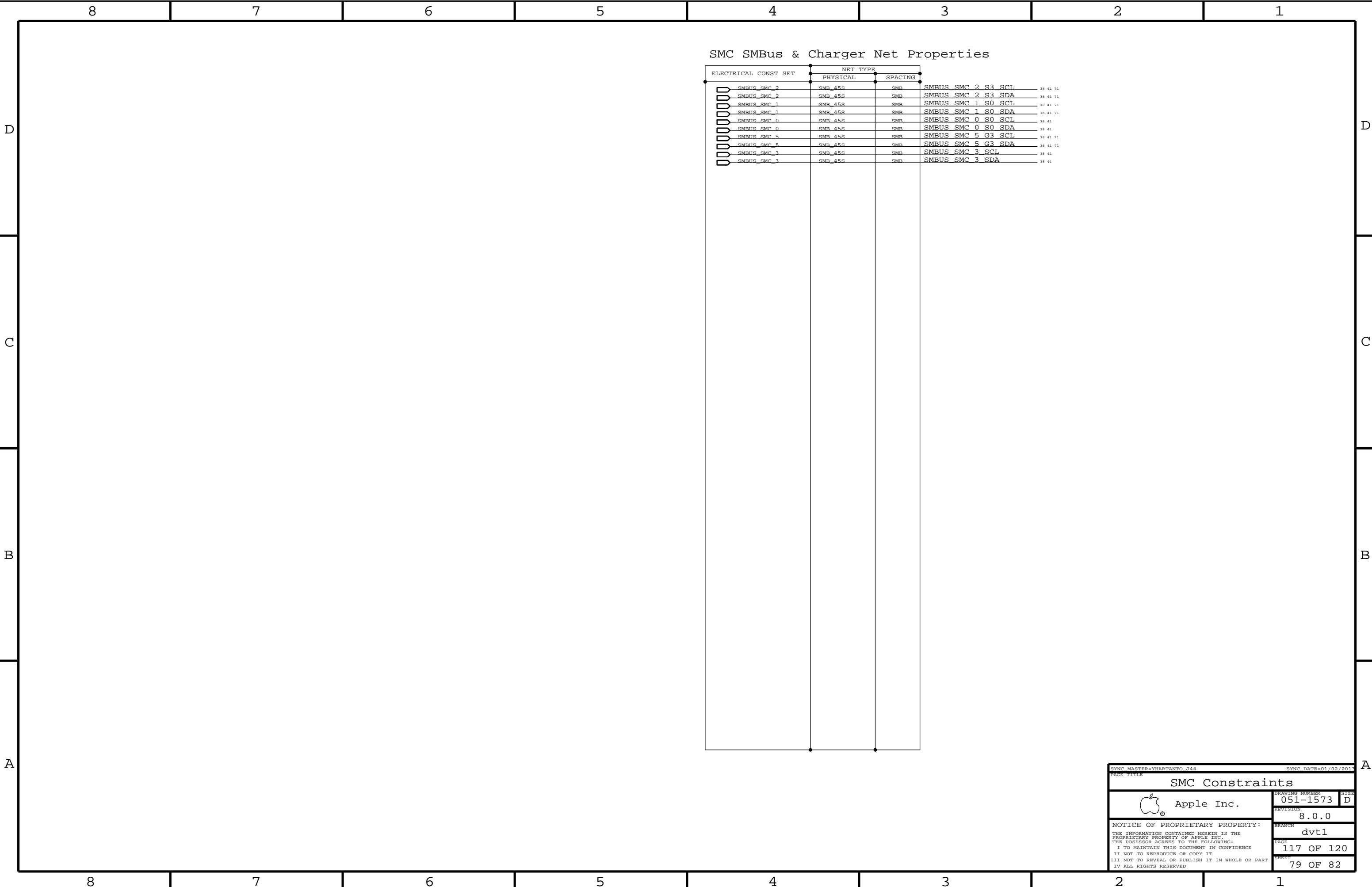
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SMC SMBus & Charger Net Properties


ELECTRICAL CONST SET	NET TYPE			
	PHYSICAL	SPACING		
 SMBUS_SMC_2	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	38 41 71
 SMBUS_SMC_2	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	38 41 71
 SMBUS_SMC_1	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	38 41 71
 SMBUS_SMC_1	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	38 41 71
 SMBUS_SMC_0	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	38 41
 SMBUS_SMC_0	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	38 41
 SMBUS_SMC_5	SMB_45S	SMB	SMBUS_SMC_5_G3_SCL	38 41 71
 SMBUS_SMC_5	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	38 41 71
 SMBUS_SMC_3	SMB_45S	SMB	SMBUS_SMC_3_SCL	38 41
 SMBUS_SMC_3	SMB_45S	SMB	SMBUS_SMC_3_SDA	38 41

SYNC MASTER=YHARTANTO J44

SYNC DATE=01/02/2013

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SMC Constraints

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SHEET

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
THERM_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
DIG_AUDIO	*	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	0.1 MM	0.1 MM
ANL_AUDIO	*	=1TO1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
ANL_AUDIO_WIDE	*	=1TO1_DIFFPAIR	0.3 MM	0.3 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	= STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	*	OVERRIDE	OVERRIDE	0.070 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S OVERRIDE	*	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	*	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.100 MM	500 MIL		
CPU_27P4S	BOTTOM			0.230 MM	100 MIL		
USB3_85D	TOP			0.100 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

DP, SATA, HDMI, PCIE CONSTRAINT RELAXATIONS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	P65_BGA
PCIE_85D	BGA	P65_BGA
CLK_PCIE_85D	BGA	P65_BGA
HDMI_85D	BGA	P65_BGA

































































NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SENSE_45S	*	SENSE_45S
THERM_45S	*	THERM_45S
DIG_AUDIO	*	DIG_AUDIO
ANL_AUDIO	*	ANL_AUDIO


X304 Specific Net Properties

ELECTRICAL CONST SET		NET TYPE		
		PHYSICAL	SPACING	
1	THERM_DP_TBT_D1	THERM_45S	THERM	TBTTHMSNS D1 P 45
1	THERM_DP_TBT_D1	THERM_45S	THERM	TBTTHMSNS D1 N 45
1	THERM_DP_CPU_D1	THERM_45S	THERM	CPUTHMSNS D1 P 45
1	THERM_DP_CPU_D1	THERM_45S	THERM	CPUTHMSNS D1 N 45
1	THERM_DP_CPU_D2	THERM_45S	THERM	CPUTHMSNS D2 P 45
1	THERM_DP_CPU_D2	THERM_45S	THERM	CPUTHMSNS D2 N 45
1				
1	SENSE_DP	SENSE_45S	SENSE	ISNS CPUDDR P 43
1	SENSE_DP	SENSE_45S	SENSE	ISNS CPUDDR N 43
1				
1	SENSE_DP_LCDBKLT	SENSE_45S	SENSE	ISNS LCDBKLT P 42 60
1	SENSE_DP_LCDBKLT	SENSE_45S	SENSE	ISNS LCDBKLT N 42 60
1	SENSE_DP_TBT	SENSE_45S	SENSE	ISNS TBT P 44
1	SENSE_DP_TBT	SENSE_45S	SENSE	ISNS TBT N 44
1	SENSE_DP	SENSE_45S	SENSE	ISNS LCDPANEL P 44 65
1	SENSE_DP	SENSE_45S	SENSE	ISNS LCDPANEL N 44 65
1				
1		SENSE_45S	SENSE	ISNS HS COMPUTING P 42 44
1		SENSE_45S	SENSE	ISNS HS COMPUTING N 42 44
1	SENSE_DP	SENSE_45S	SENSE	ISNS HS OTHER5V P 42
1	SENSE_DP	SENSE_45S	SENSE	ISNS HS OTHER5V N 42
1	SENSE_DP	SENSE_45S	SENSE	ISNS HS OTHER3V3 P 42
1	SENSE_DP	SENSE_45S	SENSE	ISNS HS OTHER3V3 N 42
1				
1	SENSE_DP_CPUVR	SENSE_45S	SENSE	CPUVR ISNS P 43
1	SENSE_DP_CPUVR	SENSE_45S	SENSE	CPUVR ISNS N 43
1	SENSE_DP_CPUVR	SENSE_45S	SENSE	CPUVR ISNS R_P 43
1	SENSE_DP_CPUVR	SENSE_45S	SENSE	CPUVR ISNS R N 43
1				
1	SENSE_DP	SENSE_45S	SENSE	ISNS 1V05_S0 P 43 59
1	SENSE_DP	SENSE_45S	SENSE	ISNS 1V05_S0 N 43 59
1	SENSE_DP	SENSE_45S	SENSE	ISNS SSD P 43
1	SENSE_DP	SENSE_45S	SENSE	ISNS SSD N 43
1	SENSE_DP	SENSE_45S	SENSE	ISNS TPAD P 42
1	SENSE_DP	SENSE_45S	SENSE	ISNS TPAD N 42
1				
1	SENSE_DP	SENSE_45S	SENSE	ISNS 1V8_S3 P 43 61
1	SENSE_DP	SENSE_45S	SENSE	ISNS 1V8_S3 N 43 61
1				
1	SENSE_DP	SENSE_45S	SENSE	ISNS PP3V3S0_P 43
1	SENSE_DP	SENSE_45S	SENSE	ISNS PP3V3S0_N 43
1	SENSE_DP	SENSE_45S	SENSE	ISNS PP5VS0_P 43
1	SENSE_DP	SENSE_45S	SENSE	ISNS PP5VS0_N 43
1				
1	SENSE_DP_CPUHIGN	SENSE_45S	SENSE	ISNS CPUHIGAIN P 44 45
1	SENSE_DP_CPUHIGN	SENSE_45S	SENSE	ISNS CPUHIGAIN N 44 45
1	SENSE_DP_CPUHIGN	SENSE_45S	SENSE	ISNS CPUHIGAIN R_P 44
1	SENSE_DP_CPUHIGN	SENSE_45S	SENSE	ISNS CPUHIGAIN R N 44
1				
1	SENSE_DP_CHGR_CST	SENSE_45S	SENSE	CHGR CSI P 54
1	SENSE_DP_CHGR_CST	SENSE_45S	SENSE	CHGR CSI N 54
1	SENSE_DP_CHGR_CST	SENSE_45S	SENSE	CHGR CSI R_P 54
1	SENSE_DP_CHGR_CST	SENSE_45S	SENSE	CHGR CSI R N 54
1	SENSE_DP_CHGR_CSO	SENSE_45S	SENSE	CHGR CSO P 54
1	SENSE_DP_CHGR_CSO	SENSE_45S	SENSE	CHGR CSO N 54
1	SENSE_DP_CHGR_CSO	SENSE_45S	SENSE	CHGR CSO R_P 44 54
1	SENSE_DP_CHGR_CSO	SENSE_45S	SENSE	CHGR CSO R N 44 54
1				
The signals below have no topologies assigned.				
1	DP_NO_TOPOLOGY	SENSE_45S	SENSE	CPUVR ISNS1_P 43 56
1	DP_NO_TOPOLOGY	SENSE_45S	SENSE	CPUVR ISNS1_N 43 56
1	DP_NO_TOPOLOGY	SENSE_45S	SENSE	CPUVR ISNS2_P 43 56
1	DP_NO_TOPOLOGY	SENSE_45S	SENSE	CPUVR ISNS2_N 43 56

The signals below have no topologies assigned.

X304 Specific Net Properties

ELECTRICAL CONST SET		NET TYPE			
		PHYSICAL	SPACING		
	AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_LQ2_L_P	48 50
	AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_LQ2_L_N	48 50
	AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_SPKRAMP_LIN_P	50
	AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_SPKRAMP_LIN_N	50
	AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	SPKRAMP_LIN_P	50
	AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	SPKRAMP_LIN_N	50
	AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_LQ2_R_P	48 50
	AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_LQ2_R_N	48 50
	AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_SPKRAMP_RIN_P	50
	AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	AUD_SPKRAMP_RIN_N	50
	AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	SPKRAMP_RIN_P	50
	AUDIO_DP_AMPTWT	ANL_AUDIO	AUDIO	SPKRAMP_RIN_N	50
	AUDIO_DP_AMPSUR	ANL_AUDIO	AUDIO	AUD_LQ3_L_P	48 50
	AUDIO_DP_AMPSUR	ANL_AUDIO	AUDIO	AUD_LQ3_L_N	48 50
	AUDIO_DP_AMPSUR	ANL_AUDIO	AUDIO	AUD_SPKRAMP_LSUBIN_P	50
	AUDIO_DP_AMPSUR	ANL_AUDIO	AUDIO	AUD_SPKRAMP_LSUBIN_N	50
	AUDIO_DP_AMPSUR	ANL_AUDIO	AUDIO	LSUBIN_P	50
	AUDIO_DP_AMPSUR	ANL_AUDIO	AUDIO	LSUBIN_N	50
	AUDIO_DP_AMESUB	ANL_AUDIO	AUDIO	AUD_LQ3_R_P	48 50
	AUDIO_DP_AMESUB	ANL_AUDIO	AUDIO	AUD_LQ3_R_N	48 50
	AUDIO_DP_AMESUB	ANL_AUDIO	AUDIO	AUD_SPKRAMP_RSUBIN_P	50
	AUDIO_DP_AMESUB	ANL_AUDIO	AUDIO	AUD_SPKRAMP_RSUBIN_N	50
	AUDIO_DP_AMESUB	ANL_AUDIO	AUDIO	RSUBIN_P	50
	AUDIO_DP_AMESUB	ANL_AUDIO	AUDIO	RSUBIN_N	50
	AUDIO_DP_SPKSUR	DTG_AUDIO	AUDIO	SPKRCONN_SL_OUT_P	50 52 71
	AUDIO_DP_SPKSUR	DTG_AUDIO	AUDIO	SPKRCONN_SL_OUT_N	50 52 71
	AUDIO_DP_SPKSUR	DTG_AUDIO	AUDIO	SPKRCONN_SR_OUT_P	50 52 71
	AUDIO_DP_SPKSUR	DTG_AUDIO	AUDIO	SPKRCONN_SR_OUT_N	50 52 71
	AUDIO_DP_SPKTWT	DTG_AUDIO	AUDIO	SPKRCONN_L_OUT_P	50 52 71
	AUDIO_DP_SPKTWT	DTG_AUDIO	AUDIO	SPKRCONN_L_OUT_N	50 52 71
	AUDIO_DP_SPKTWT	DTG_AUDIO	AUDIO	SPKRCONN_R_OUT_P	50 52 71
	AUDIO_DP_SPKTWT	DTG_AUDIO	AUDIO	SPKRCONN_R_OUT_N	50 52 71
	AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CH_HS_GND	48 52
	AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_HS_MIC_P	
	AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_SLEEVE	52
	AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_SLEEVE_XW	51 52
	AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_HP_PORT_REFCH	48 52
	AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_HS_MIC_P	51 52
	AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	CODEC_HS_MIC_P	48
	AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	HS_MIC_P	48 51
	AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_HS_MIC_N	
	AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_RING2	52
	AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_CONN_RING2_XW	51 52
	AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_HP_PORT_REFUS	48 52
	AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_HS_MIC_N	51 52
	AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	AUD_US_HS_GND	48 52
	AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	HS_MIC_N	48 51
	AUDIO_DP_MIC	ANL_AUDIO_WIDE	AUDIO	CODEC_HS_MIC_N	48
					
			SR_POWER	PP3V3_S5	68 71
			SR_POWER	PP3V3_S0	68 71
					
					
					
					
					
					
					
					
					
					
					
					
					

SYNC MASTER=VHARTANTO J44		SYNC DATE=01/04/2013	
PAGE TITLE			
Project Specific Constraints			
 Apple Inc.		DRAWING NUMBER	051-1573
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PCI Express Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=3X_DIELECTRIC	?	PCIE_2SAME	TOP, BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?	PCIE_TXRX	TOP, BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?	PCIE_2OTHER	TOP, BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?	PCIE_2CLK	TOP, BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?	PCIECLK_2OTHER	TOP, BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER
PCIE_TX	*_RX	*	PCIE_TXRX
PCIE_RX	*_TX	*	PCIE_TXRX

PCI Express Properties

ELECTRICAL CONST SET		NET TYPE			
		PHYSICAL	SPACING		
	PCIE SSD D2R	PCIE_85D	PCIE_RX	PCIE SSD D2R P<3..1>	12 32 71
	PCIE SSD D2R	PCIE_85D	PCIE_RX	PCIE SSD D2R N<3..1>	12 32 71
	PCIE SSD D2R_PP	PCIE_85D	PCIE_RX	PCIE SSD D2R P<0>	12 32 71
	PCIE SSD D2R_PP	PCIE_85D	PCIE_RX	PCIE SSD D2R N<0>	12 32
	PCIE SSD R2D	PCIE_85D	PCIE_TX	PCIE SSD R2D C P<3..0>	12 32 71
	PCIE SSD R2D	PCIE_85D	PCIE_TX	PCIE SSD R2D C N<3..0>	12 32 71
	PCIE SSD R2D	PCIE_85D	PCIE_TX	PCIE SSD R2D P<3..0>	32 71
	PCIE SSD R2D	PCIE_85D	PCIE_TX	PCIE SSD R2D N<3..0>	32 71
	PCIE TBT D2R_0	PCIE_85D	PCIE_RX	PCIE TBT D2R P<0>	14 25 71
	PCIE TBT D2R_0	PCIE_85D	PCIE_RX	PCIE TBT D2R N<0>	14 25 71
	PCIE TBT D2R_0	PCIE_85D	PCIE_RX	PCIE TBT D2R C P<0>	25
	PCIE TBT D2R_0	PCIE_85D	PCIE_RX	PCIE TBT D2R C N<0>	25
	PCIE TBT D2R	PCIE_85D	PCIE_RX	PCIE TBT D2R P<3..1>	14 25 71
	PCIE TBT D2R	PCIE_85D	PCIE_RX	PCIE TBT D2R N<3..1>	14 25 71
	PCIE TBT D2R	PCIE_85D	PCIE_RX	PCIE TBT D2R C P<3..1>	25 71
	PCIE TBT D2R	PCIE_85D	PCIE_RX	PCIE TBT D2R C N<3..1>	25 71
	PCIE TBT R2D	PCIE_85D	PCIE_TX	PCIE TBT R2D P<3..0>	25 71
	PCIE TBT R2D	PCIE_85D	PCIE_TX	PCIE TBT R2D N<3..0>	25 71
	PCIE TBT R2D	PCIE_85D	PCIE_TX	PCIE TBT R2D C P<3..0>	14 25 71
	PCIE TBT R2D	PCIE_85D	PCIE_TX	PCIE TBT R2D C N<3..0>	14 25 71
	PCIE AP R2D	PCIE_85D	PCIE_TX	PCIE AP R2D P	66 71
	PCIE AP R2D	PCIE_85D	PCIE_TX	PCIE AP R2D N	66 71
	PCIE AP R2D	PCIE_85D	PCIE_TX	PCIE AP R2D C P	14 66 71
	PCIE AP R2D	PCIE_85D	PCIE_TX	PCIE AP R2D C N	14 66 71
	PCIE AP D2R	PCIE_85D	PCIE_RX	PCIE AP D2R P	14 66 71
	PCIE AP D2R	PCIE_85D	PCIE_RX	PCIE AP D2R N	14 66 71
	PCIE CLK100M AP	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M AP CONN P	66
	PCIE CLK100M AP	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M AP CONN N	66
	PCIE CLK100M AP	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M AP P	12 66 71
	PCIE CLK100M AP	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M AP N	12 66 71
	PCIE CLK100M CAM	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA P	12 34 71
	PCIE CLK100M CAM	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA N	12 34 71
	PCIE CLK100M CAM	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA C P	33 34
	PCIE CLK100M CAM	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M CAMERA C N	33 34
	PCIE CLK100M SSD	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M SSD P	12 32 71
	PCIE CLK100M SSD	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M SSD N	12 32 71
	PCIE CLK100M SSD	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M SSD RC1 P	32
	PCIE CLK100M SSD	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M SSD RC1 N	32
	PCIE CLK100M SSD	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M SSD RC2 P	32
	PCIE CLK100M SSD	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M SSD RC2 N	32
	PCIE CLK100M TBT	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M TBT P	12 25 71
	PCIE CLK100M TBT	CLK_PCIE_85D	CLK_PCIE	PCIE CLK100M TBT N	12 25 71
	PCIE CAMERA D2R	PCIE_85D	PCIE_RX	PCIE CAMERA D2R P	14 34 71
	PCIE CAMERA D2R	PCIE_85D	PCIE_RX	PCIE CAMERA D2R N	14 34 71
	PCIE CAMERA D2R	PCIE_85D	PCIE_RX	PCIE CAMERA D2R C P	33 34
	PCIE CAMERA D2R	PCIE_85D	PCIE_RX	PCIE CAMERA D2R C N	33 34
	PCIE CAMERA R2D	PCIE_85D	PCIE_TX	PCIE CAMERA R2D P	33 34
	PCIE CAMERA R2D	PCIE_85D	PCIE_TX	PCIE CAMERA R2D N	33 34
	PCIE CAMERA R2D	PCIE_85D	PCIE_TX	PCIE CAMERA R2D C P	14 34
	PCIE CAMERA R2D	PCIE_85D	PCIE_TX	PCIE CAMERA R2D C N	14 34


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D	<div>Change List: <RDAR://COMPONENT/XXXXXX> X304 HW EE SCHEMATIC PROTO 0</div> <div>Kismet: AFP://KISMET.APPLE.COM/KISMET-PROJECTS/X304</div> <div>Useful Wiki Links: Schematic Conventions - https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions Schematic Design Wiki - https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design</div> <div>MobileMac HW Radar: <rdar://component/497591> MobileMac HW Task <rdar://component/497587> MobileMac HW Schematic <rdar://component/497585> MobileMac HW New Bugs <rdar://component/497588> MobileMac HW Layout <rdar://component/497590> MobileMac HW Investigation <rdar://component/497589> MobileMac HW Architecture</div> <div>Other Info: Page Allocations - <rdar://problem/11791318> 2012 Schematic Page Allocations</div>								D
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